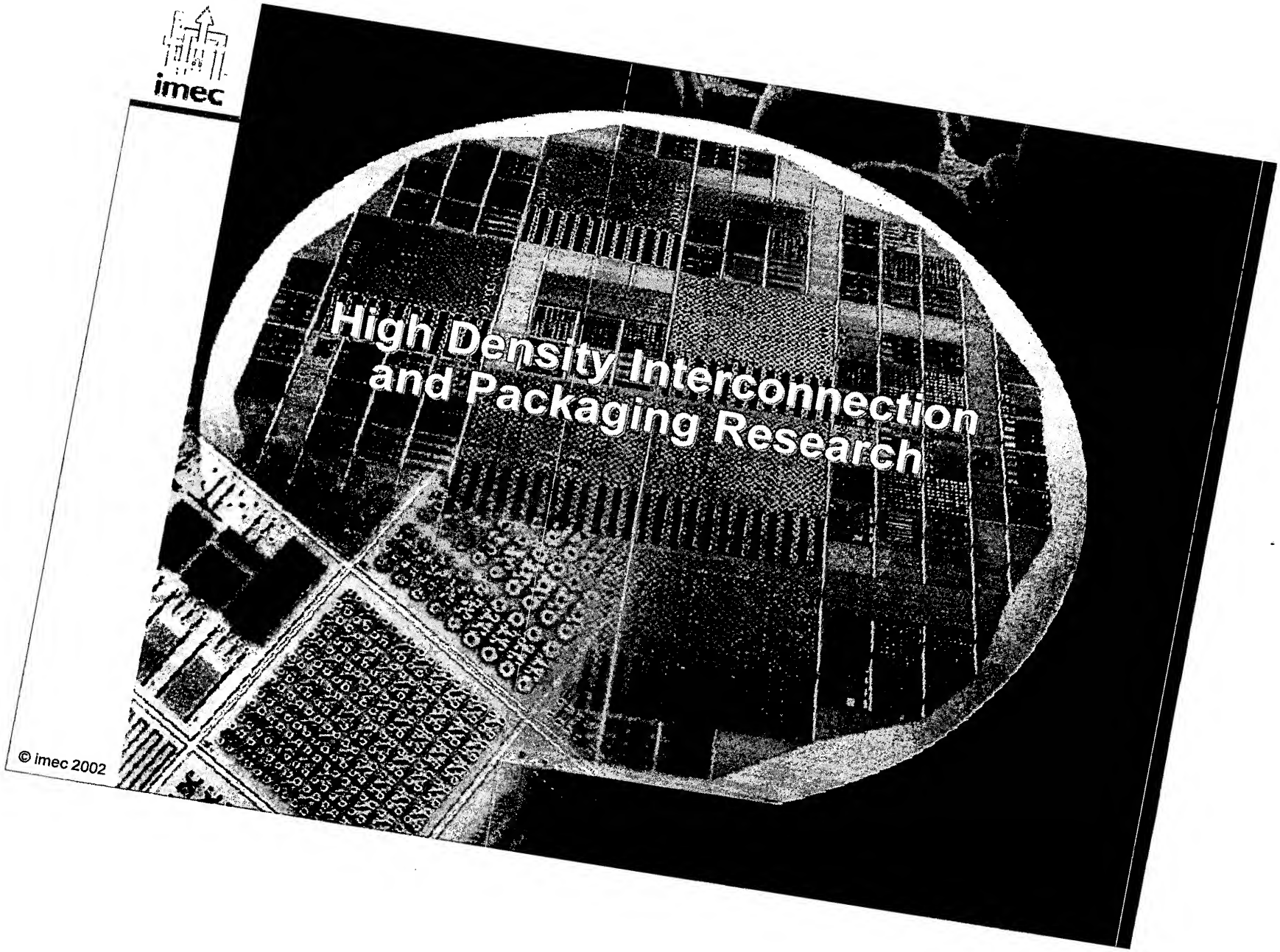
imec

Enabling Technologies for Distributed and Autonomous Electronic Systems, EDAS

E.Beyne

J.Poortmans

SEEDS FOR TOMORROW'S WORLD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High Density Interconnection and Packaging Research
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Requirements for High Density Interconnect and Assembly technologies

Drivers from IC technology roadmaps

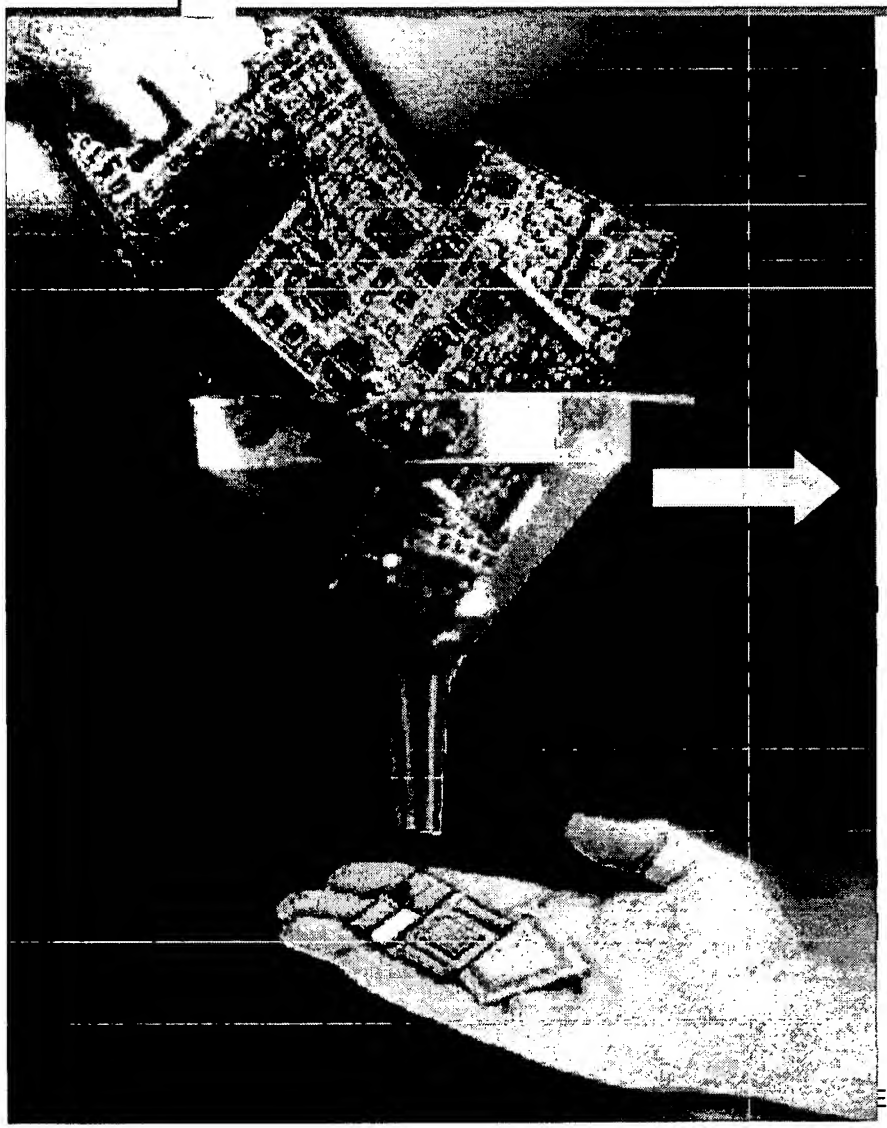
- High I/O density (more I/O's on smaller area)
- New materials : Cu/low k
- High speed (digital & rf), high power
- Integration enables "System on chip", SOC

Drivers from System roadmaps

- Divergence among Si-technologies : high density logic (CMOS), Memory, Analog, rf, MEMS,....
- Systems consist of many non-silicon components : Passives, Displays, sensors, antennas, connectors, ...
- ⑤ "System-in-a-Package", SIP = *Multiple components on a high density interconnect substrate, realizing a (sub)-system function*

SOC or SIP ? Because of SOC, (sub)systems may be miniaturised to the scale of a SIP package

Miniaturisation of Electronic Systems



Enabling Technologies :

- Si-integration : SOC
- High Density Interconnection technologies

  SIP – "System-in-a-package"

Positioning EDAS in R&D HDIP

IMEC core competences :

- Thin film lithography
- Planar technology
- Wafer level processing
- "IC-centric"approach

Associated lab Gent : "PCB-centric" interconnect and assembly technology

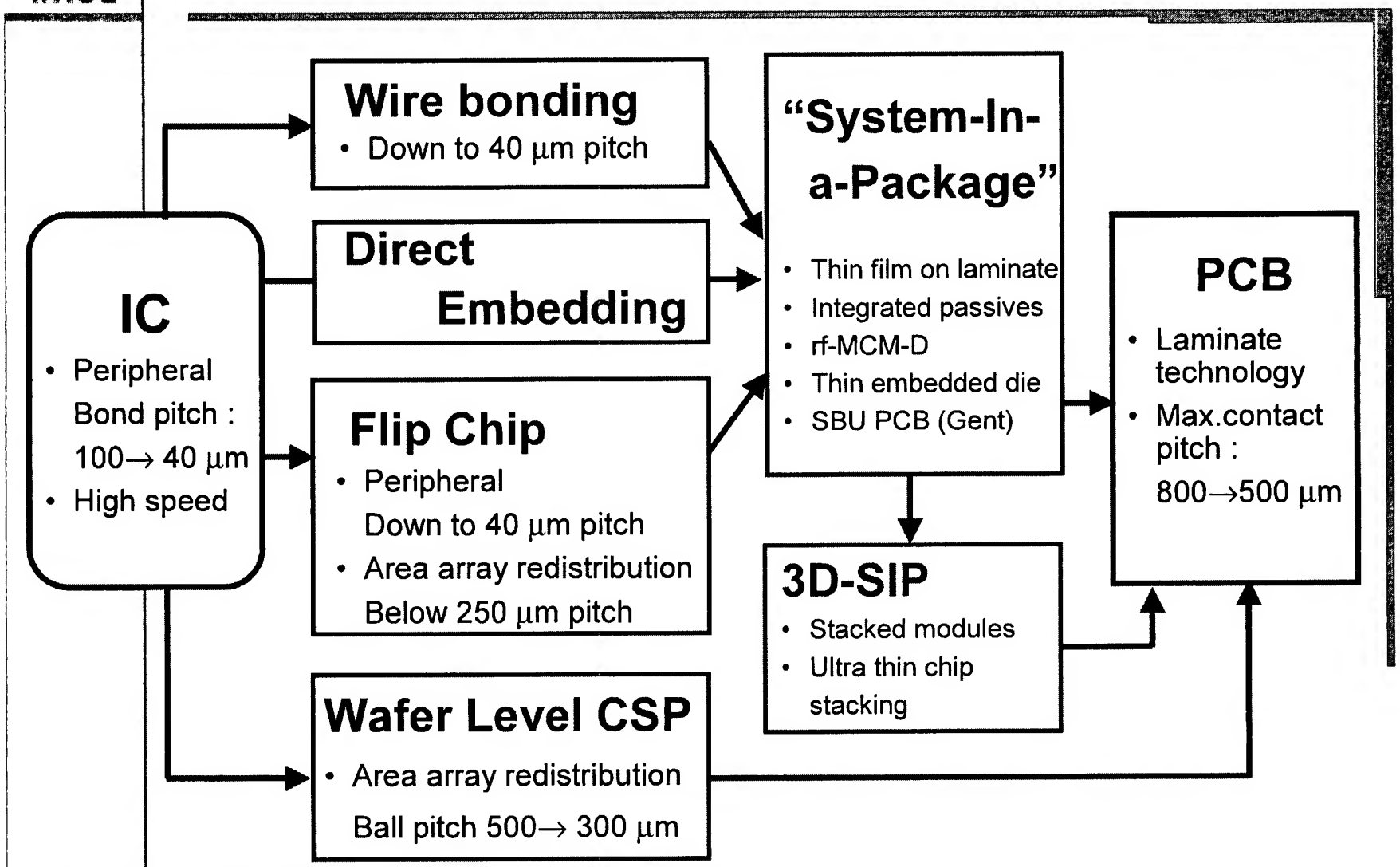
Interconnect & packaging needs are key element IMEC/MCP Strategic R&D Programs :

M4, Human++, heterogeneous integration, Power systems

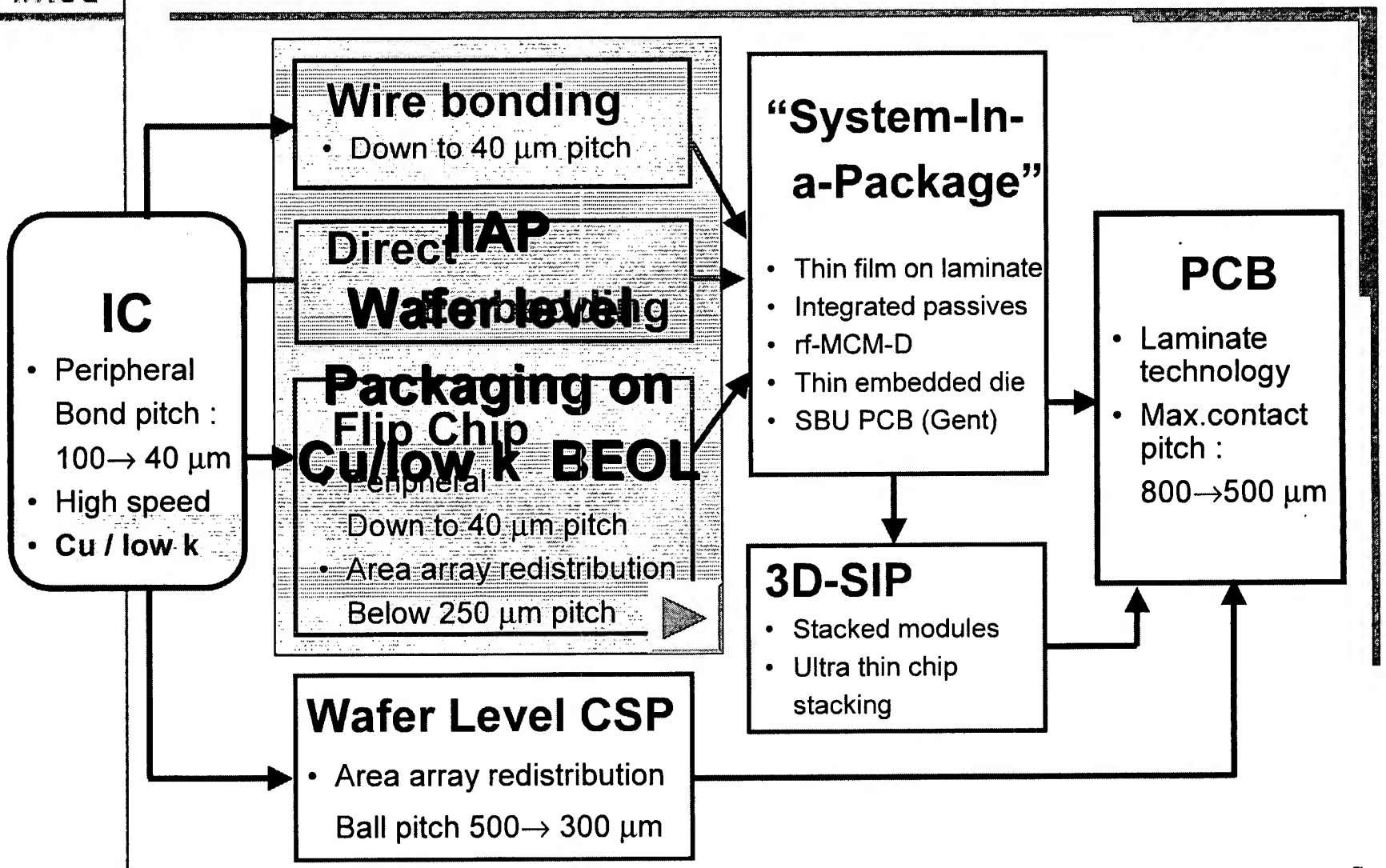
Therefore :

- *Baseline technology : low temperature "multilayer thin film technology"*
- *High density chip interconnects : ultra-fine pitch wire bonding & flip chip bumping & assembly*
- *3D-integration : stacking of SIP and bare die*

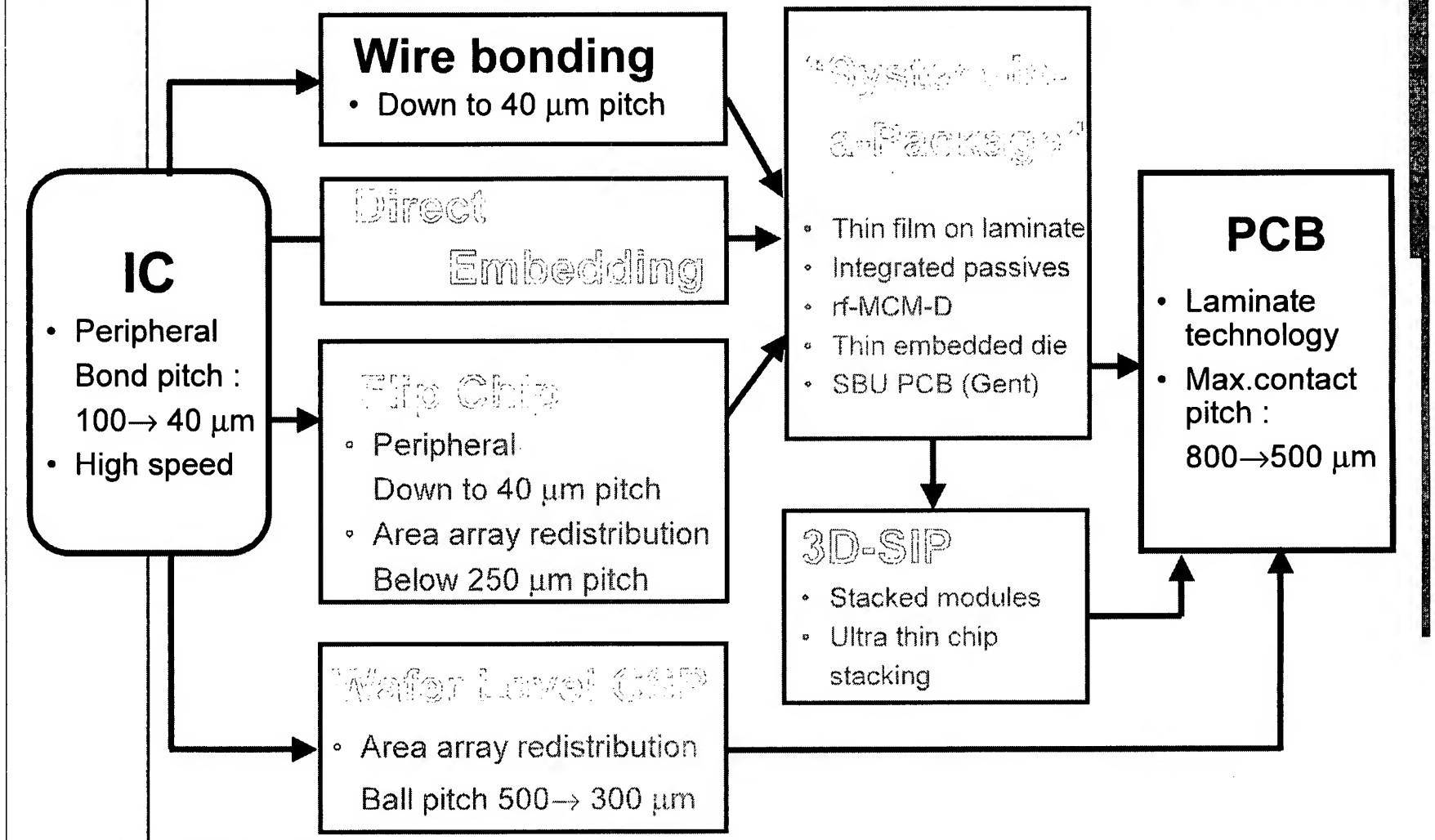
Connecting high density IC's



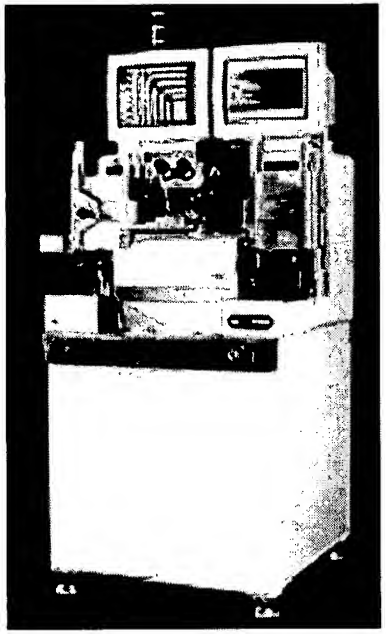
Connecting high density IC's



Connecting high density IC's



Advanced Wire bonding



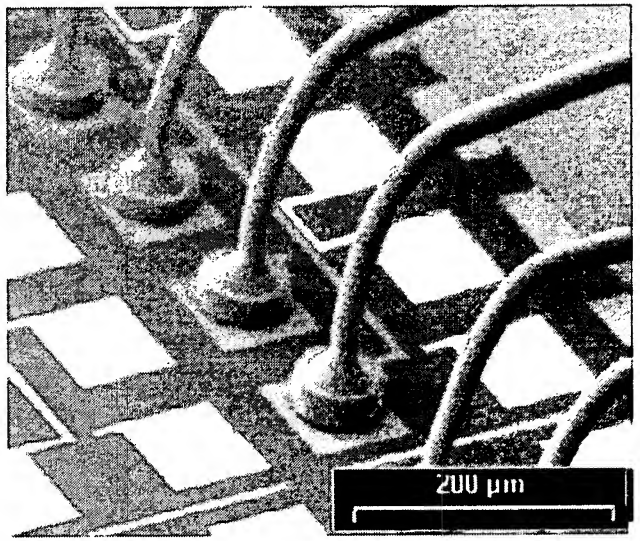
AB 339 Eagle

- 138 kHz US generator
- Ultra Fine Pitch Bonding (down to 30µm)
- Au & Cu Wire capable
- tailless bumping

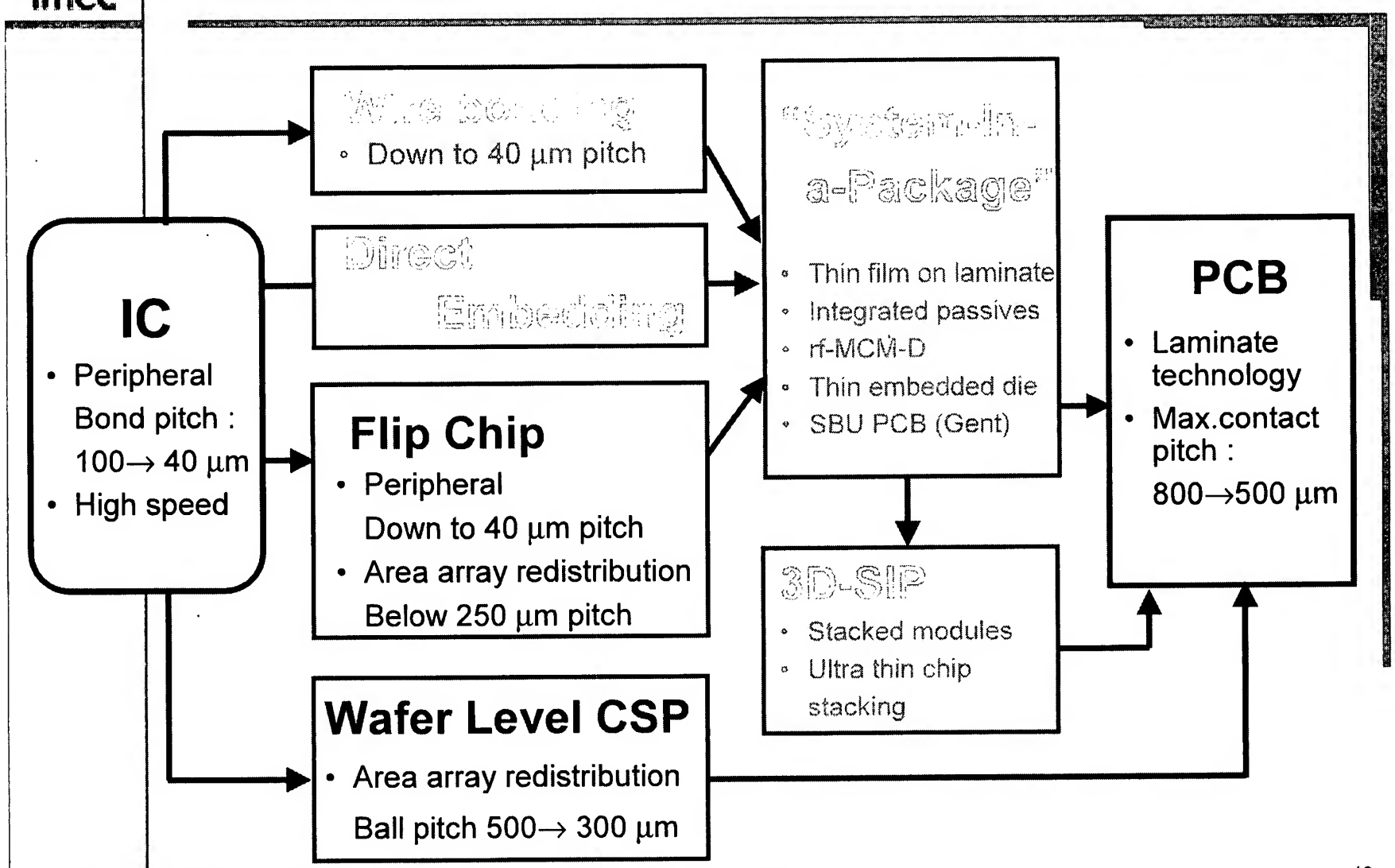
WLP-IIAP with ASM Pacific :

- Fine pitch, down to 40 µm, Au and Cu wire bonding to Cu/low k chips
- Direct wire bonding to organic-coated Cu pads

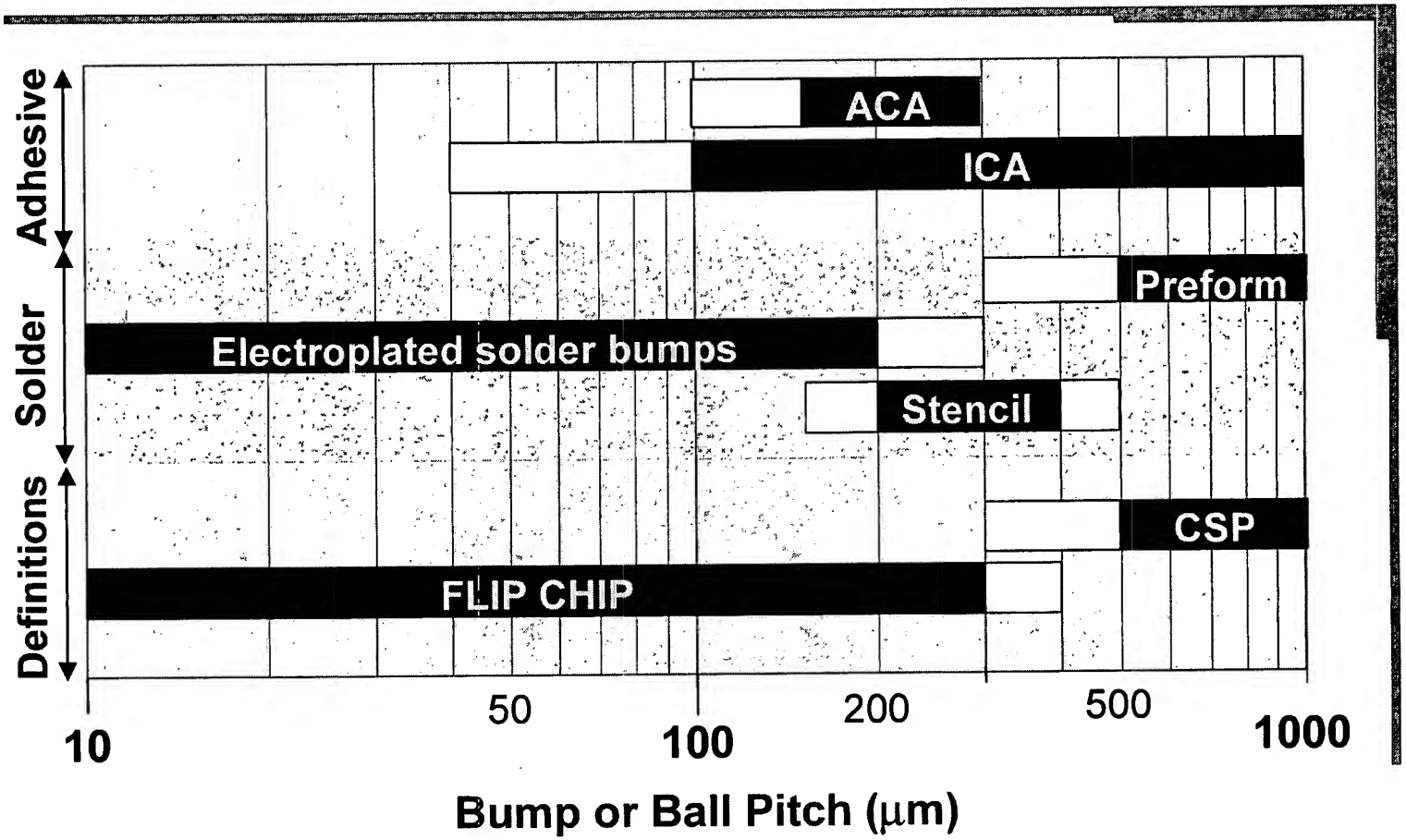
⑤ *Use of SAM organic protective coating key to bonding success*



Connecting high density IC's



"Flip chip" technologies

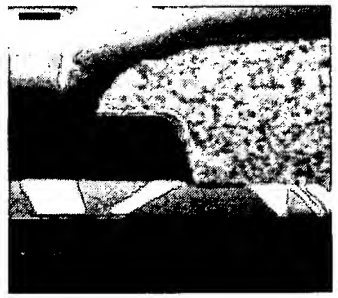


Main focus : electroplating of solder bumps

Flip Chip Technology Strategy

Under-bump metallurgy,UBM : (barrier + solderable layer)

- Electrolytic plating 3µm Cu / 3µm Ni + solder
- Electroless plating 3µm Ni:P / 150 nm Au
- PVD : diffusion barier + non reactive seed layer

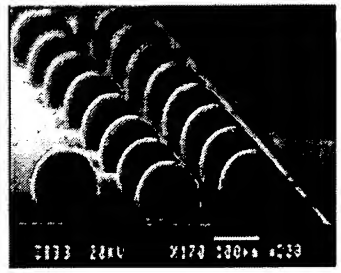


Chip I/O-pitch > 200 µm :

- Solder bumping by screen printing solder paste

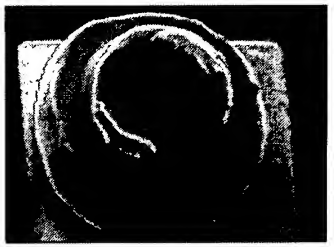
Chip I/O-pitch < 200 µm :

- **Electroplated solder** bumps :
  - Baseline : Eutectic SnPb
  - lead-free solder : **Sn(Cu), SnAg(Cu), AuSn**
- **Thin film redistribution** to larger pitches

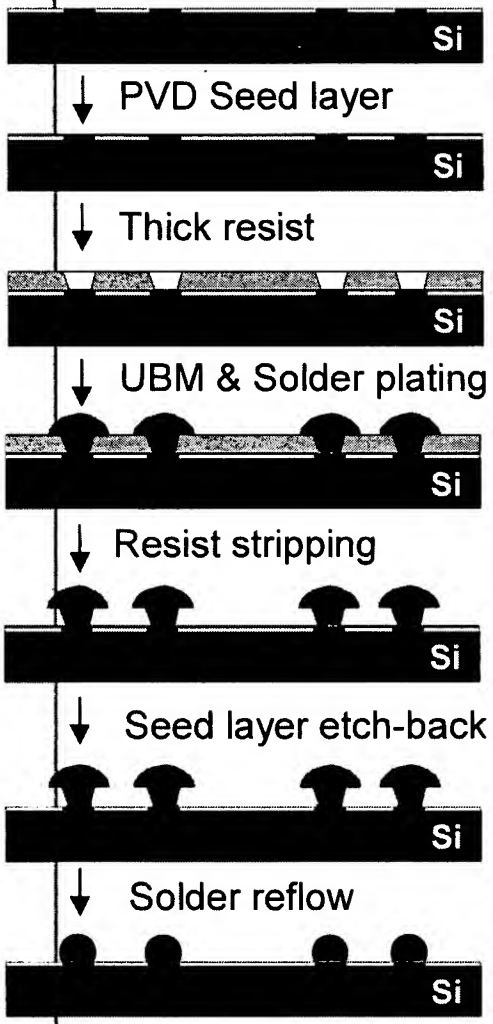


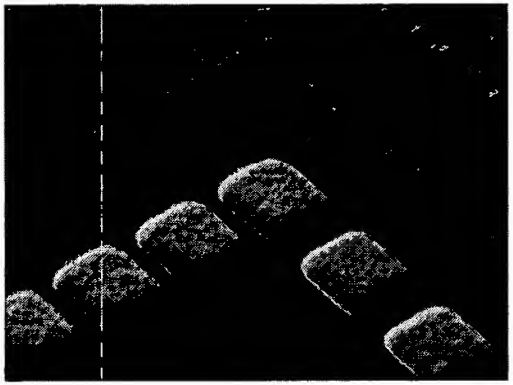
Prototyping, small series :

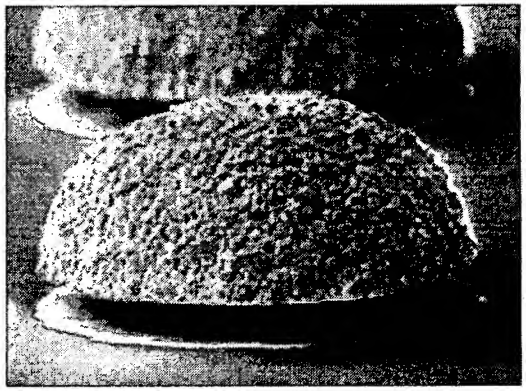
- Stud bumps realised using ball bonding equipment :
  - Au thermo-compression or adhesive bonding
  - Cu stud bumps with solder joining

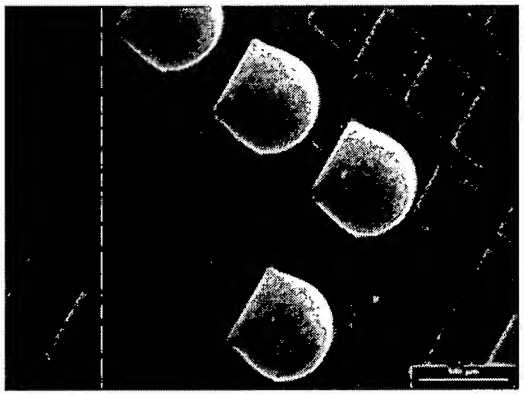


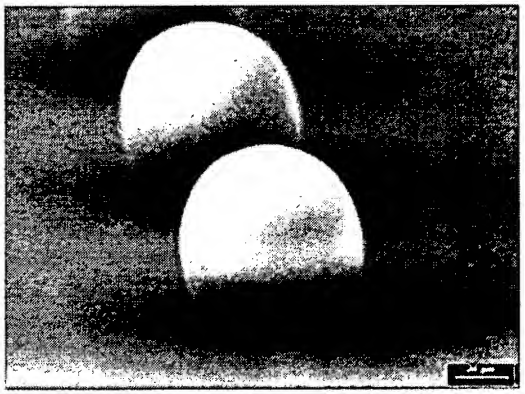
Electroplated solder bumping







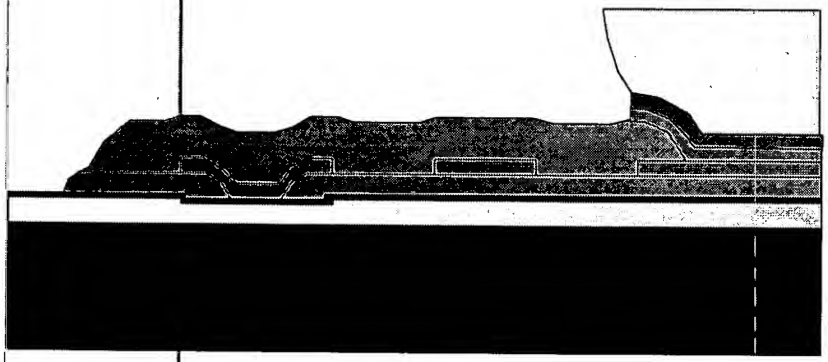




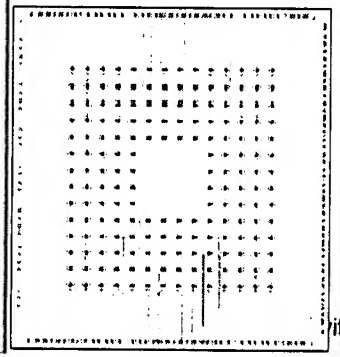
Wafer Level Pad Redistribution for flip chip and wafer level CSP

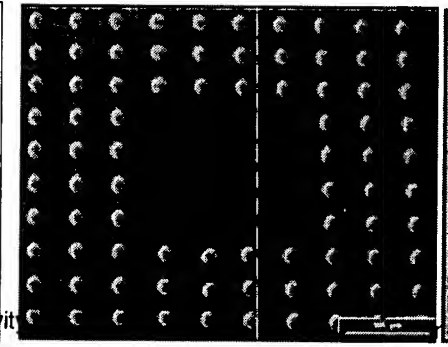
Flip chip redistribution

Solder balls <100 μm



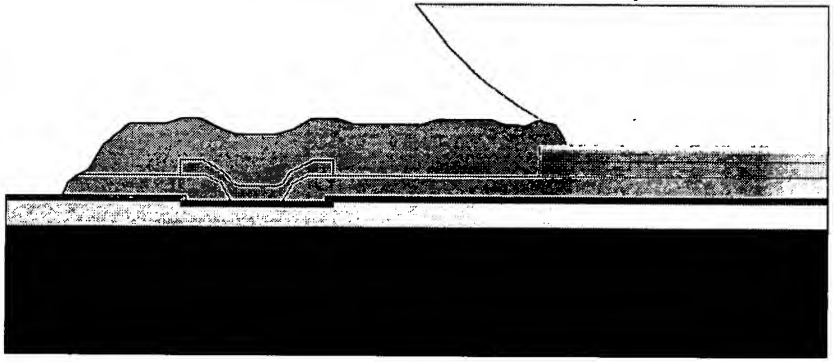
- Si wafer
- Cu/low K interconnect
- Cu bond pad
- Chip passivation
- BCB Dielectric
- Electroplated Cu
- Electroplated Ni (UBM)
- Electroplated solder bump



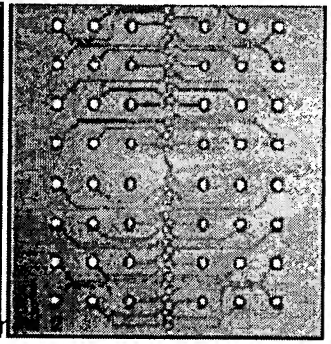


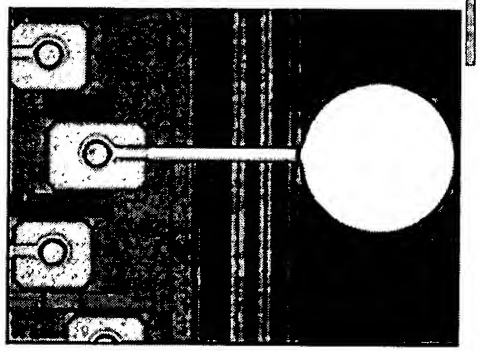
Wafer level CSP

Solder balls >300 μm

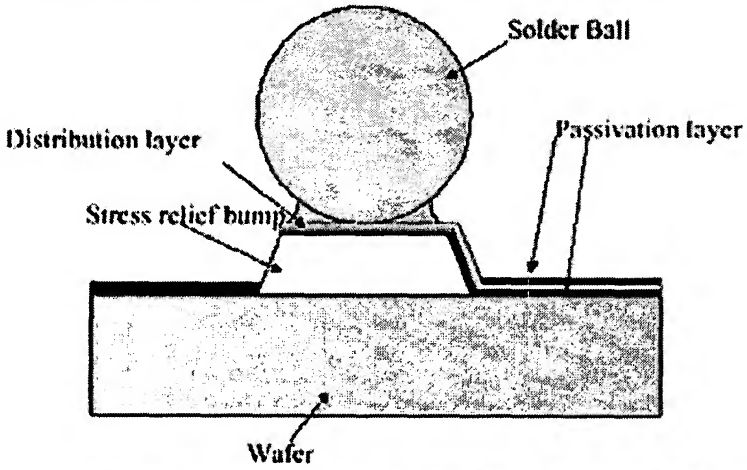


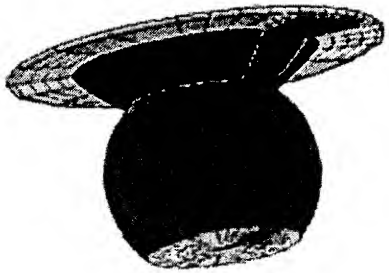
- Si wafer
- Cu/low K interconnect
- Cu bond pad
- Chip passivation
- Dielectric (BCB)
- Electroplated Cu
- Electroplated Ni (UBM)
- Electroplated Au
- Preform solder ball





Wafer level CSP with compliant layer below the solder ball





Structure optimisation
By FEM modeling

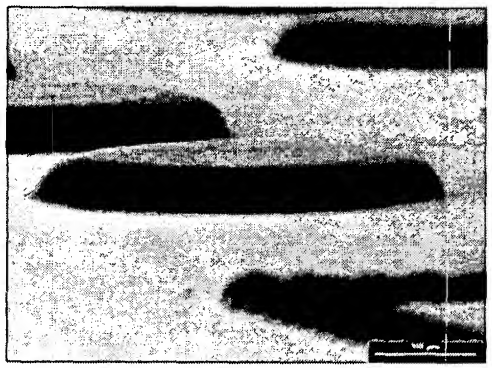
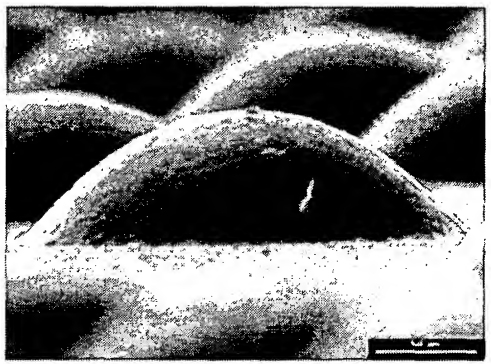


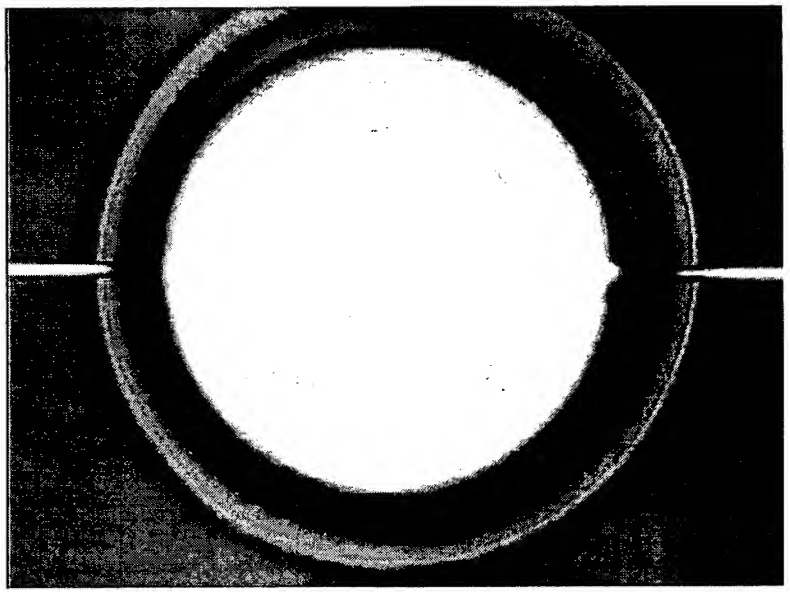
Photo-defined
Silicone bumps



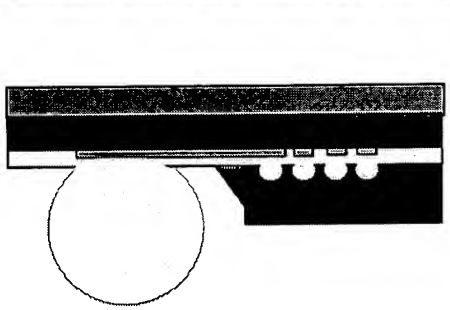
Screen printed
Silicone bumps

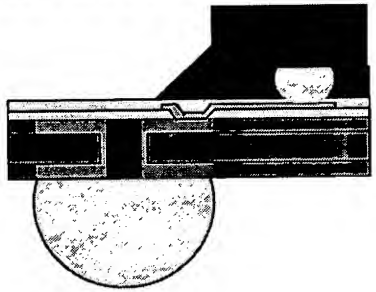
DOW CORNING

Bump metallization (non optimised design)

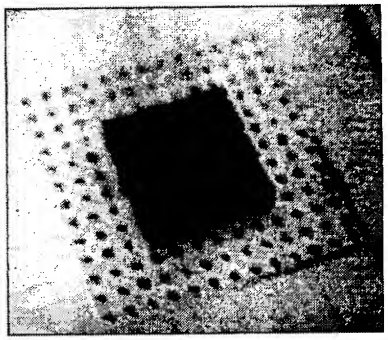


Thin film Interposer technology

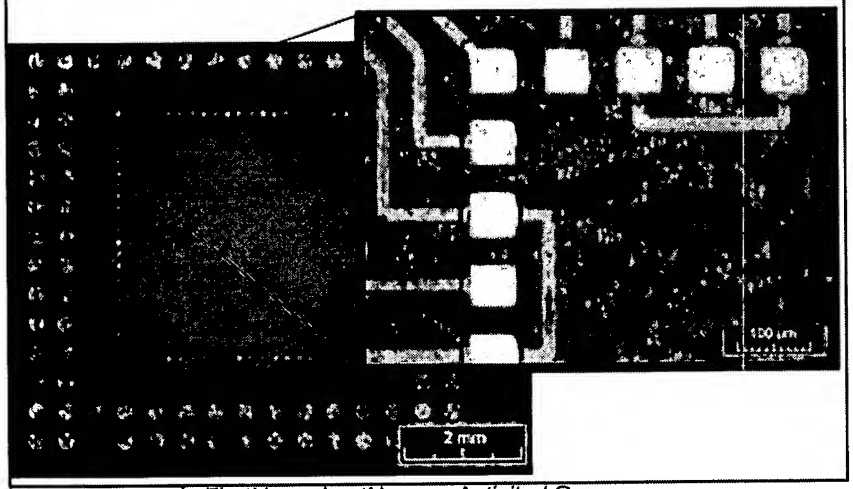


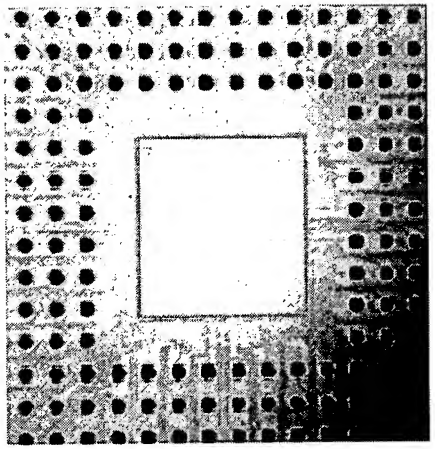


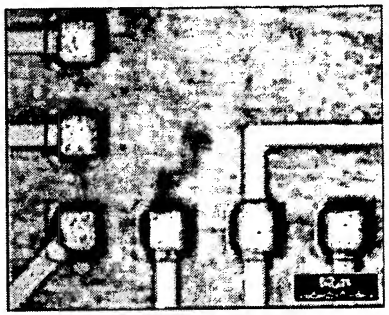
Thin film Redistribution process on on laminate substrate



on AlSi substrate

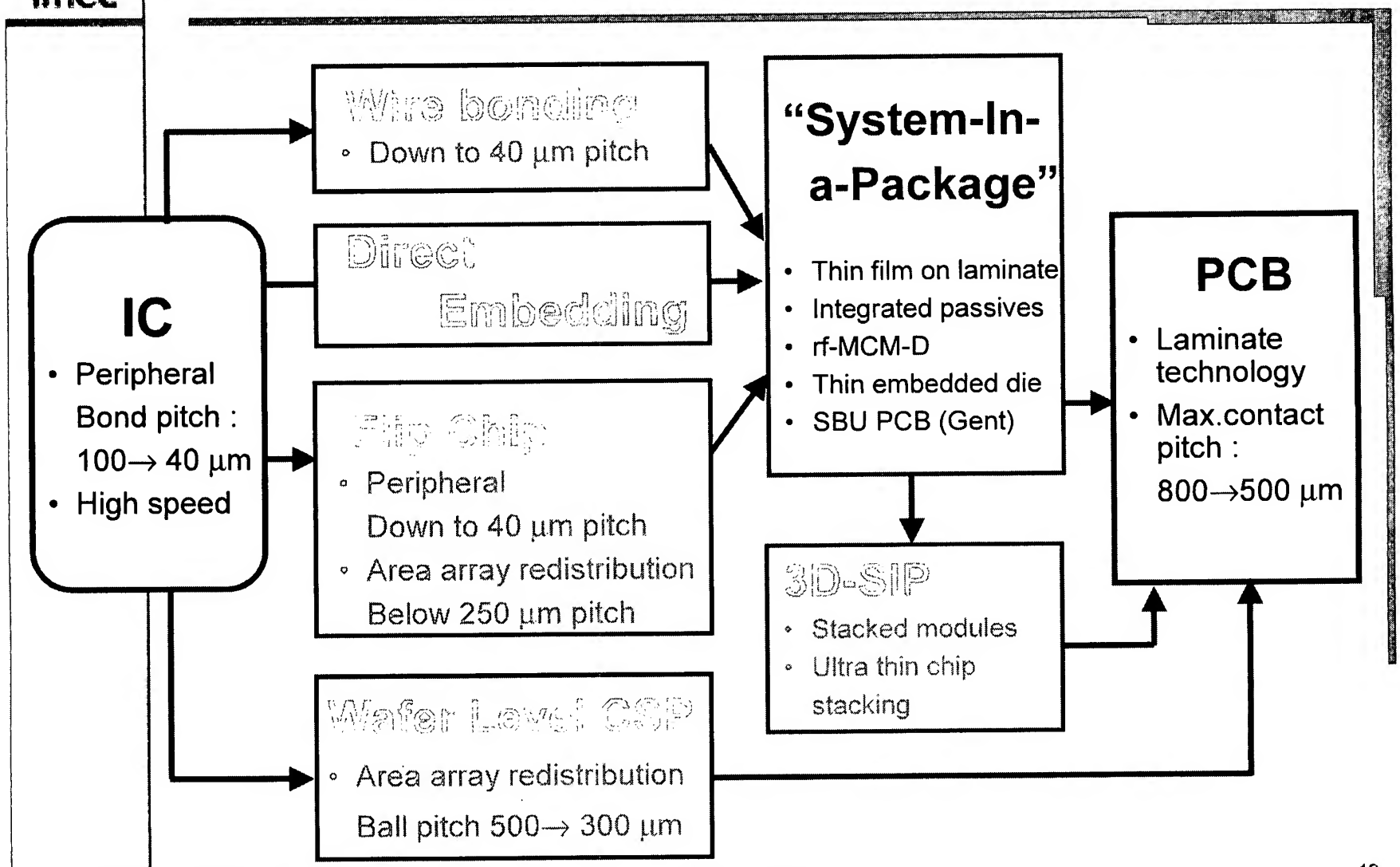






60 µm flip chip bump pitch

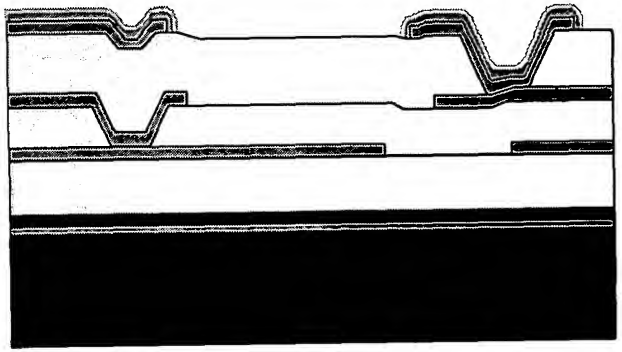
Connecting high density IC's



High Density Thin Film Interconnects for Digital Applications

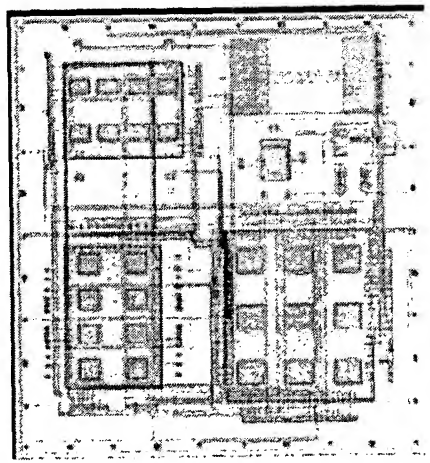
Technology :

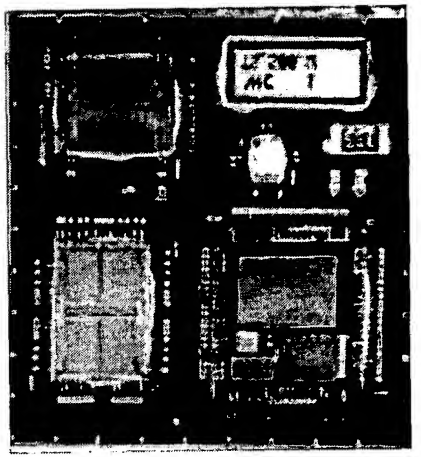
- **Substrates : 150 mm Ø, Si, glass, ceramic, high Tg laminate or metal.**
- **BCB spin-on photosensitive dielectric layers**
- **Cu lines, 3-5μm thick, down to 10μm wide lines & spaces**
- **Metal finish top surface : Cu/Ni/Au**
- **Power & ground layers : 2 μm thick Al**
- **Integrated decoupling capacitors (0.75 nF/mm^2)**



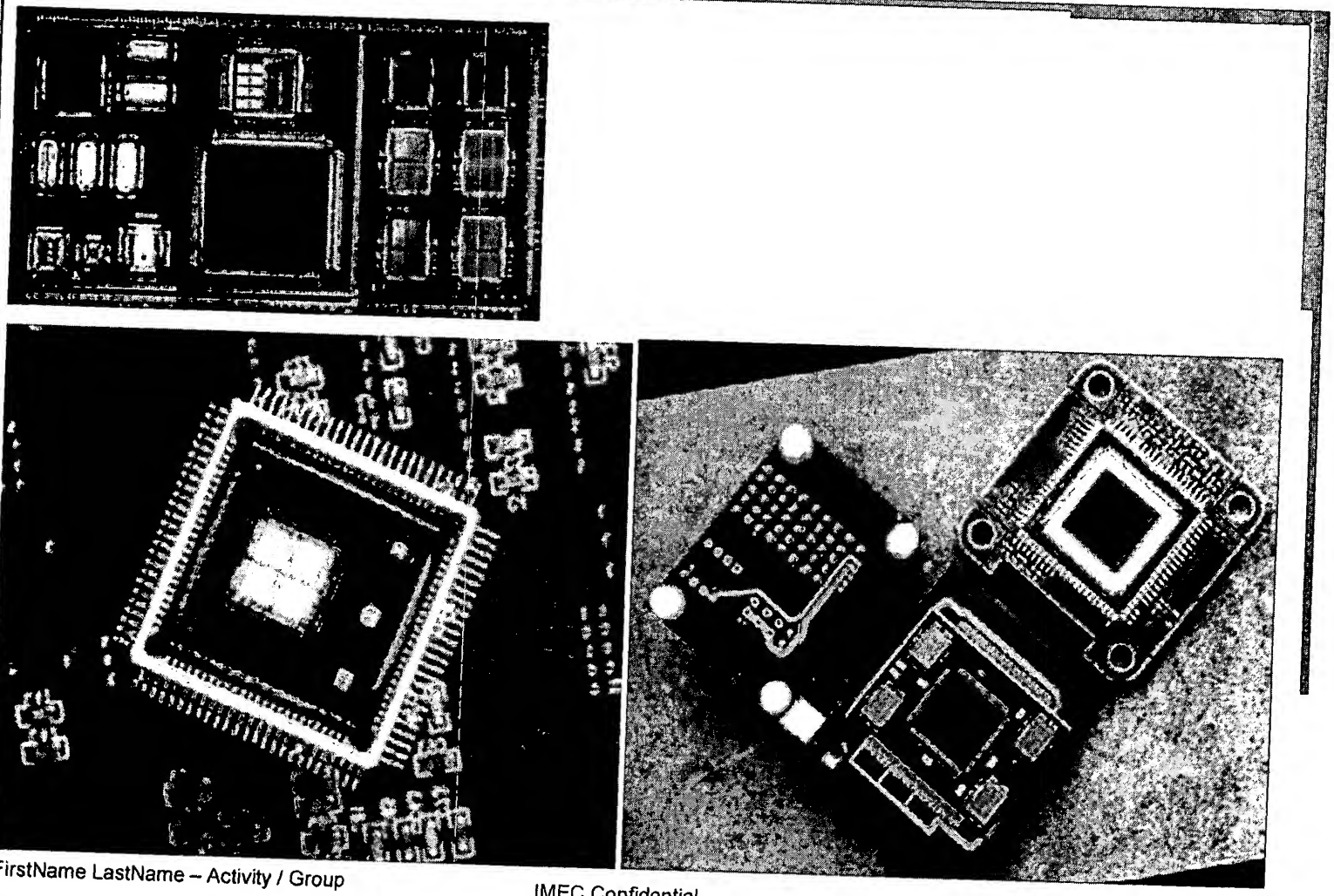
Design :

- "Manhattan" style X-Y routing,
- Automated design methodology

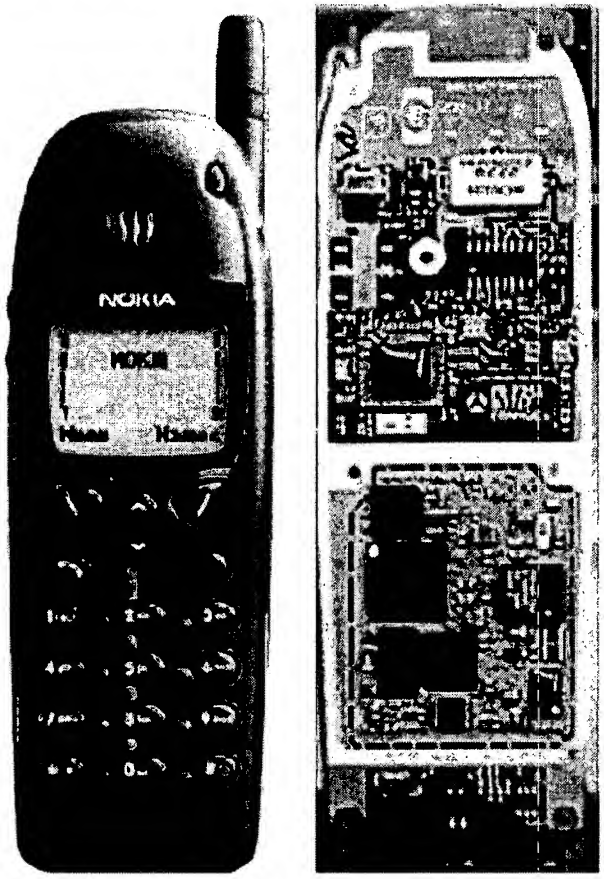


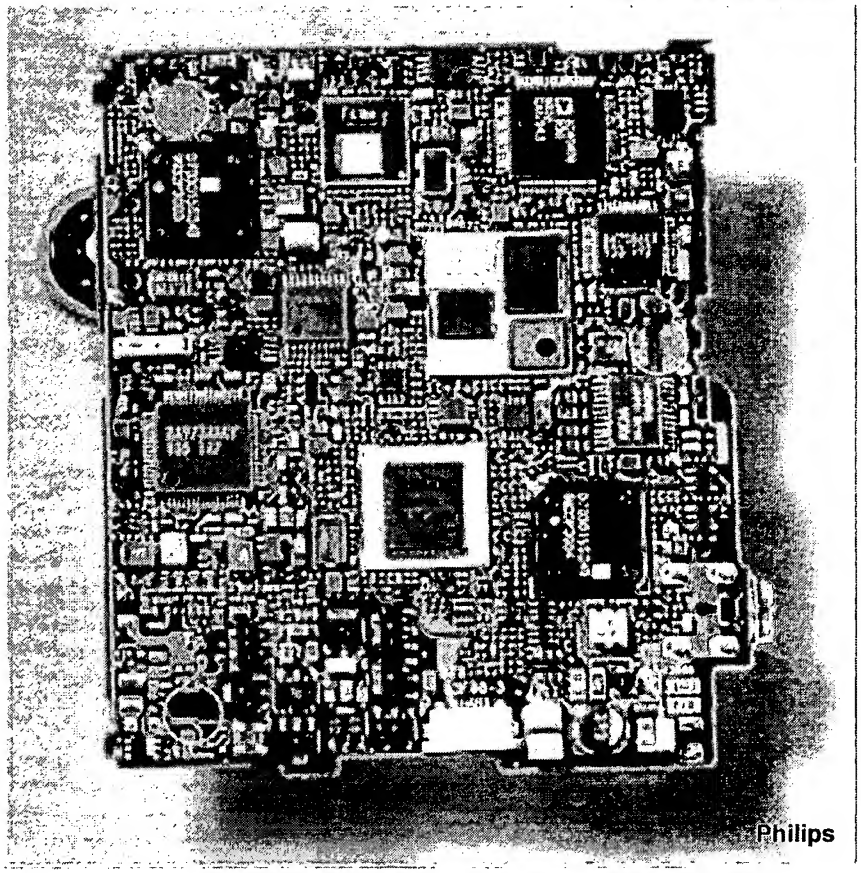


Thin Film Digital Multi-chip Modules



Current Electronic systems



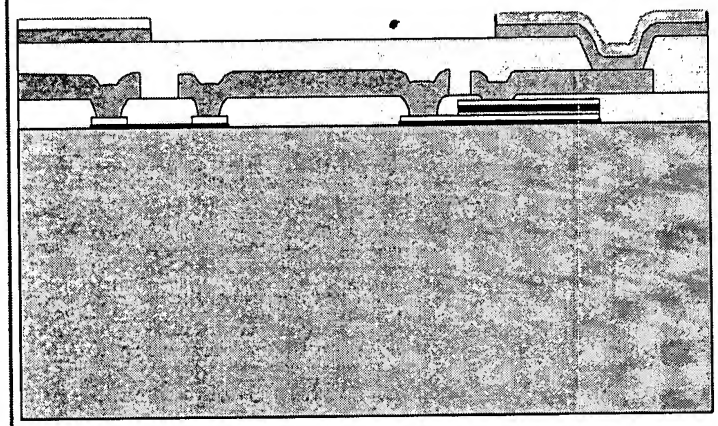


High component count & Large variety of technologies

Majority of components : passives

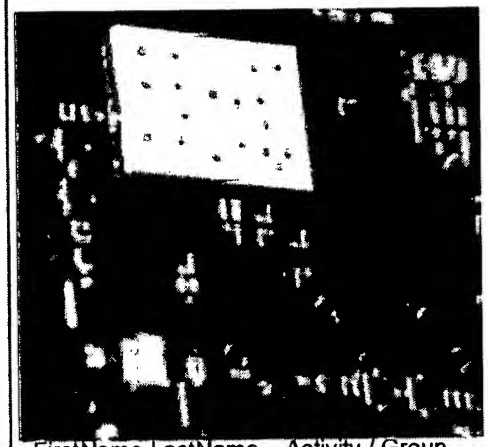
Many non-silicon components : displays, key-pad, connectors …

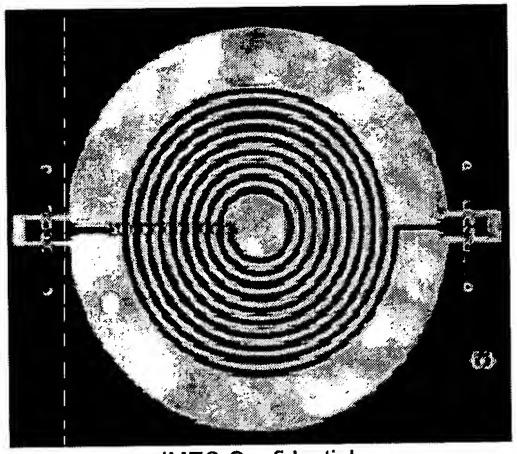
Multilayer Thin Film with Integrated Passives

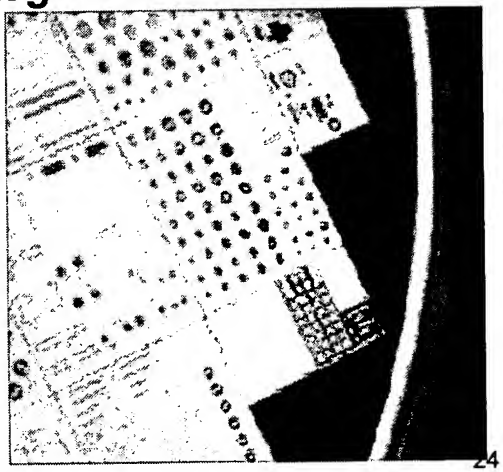


Main features :

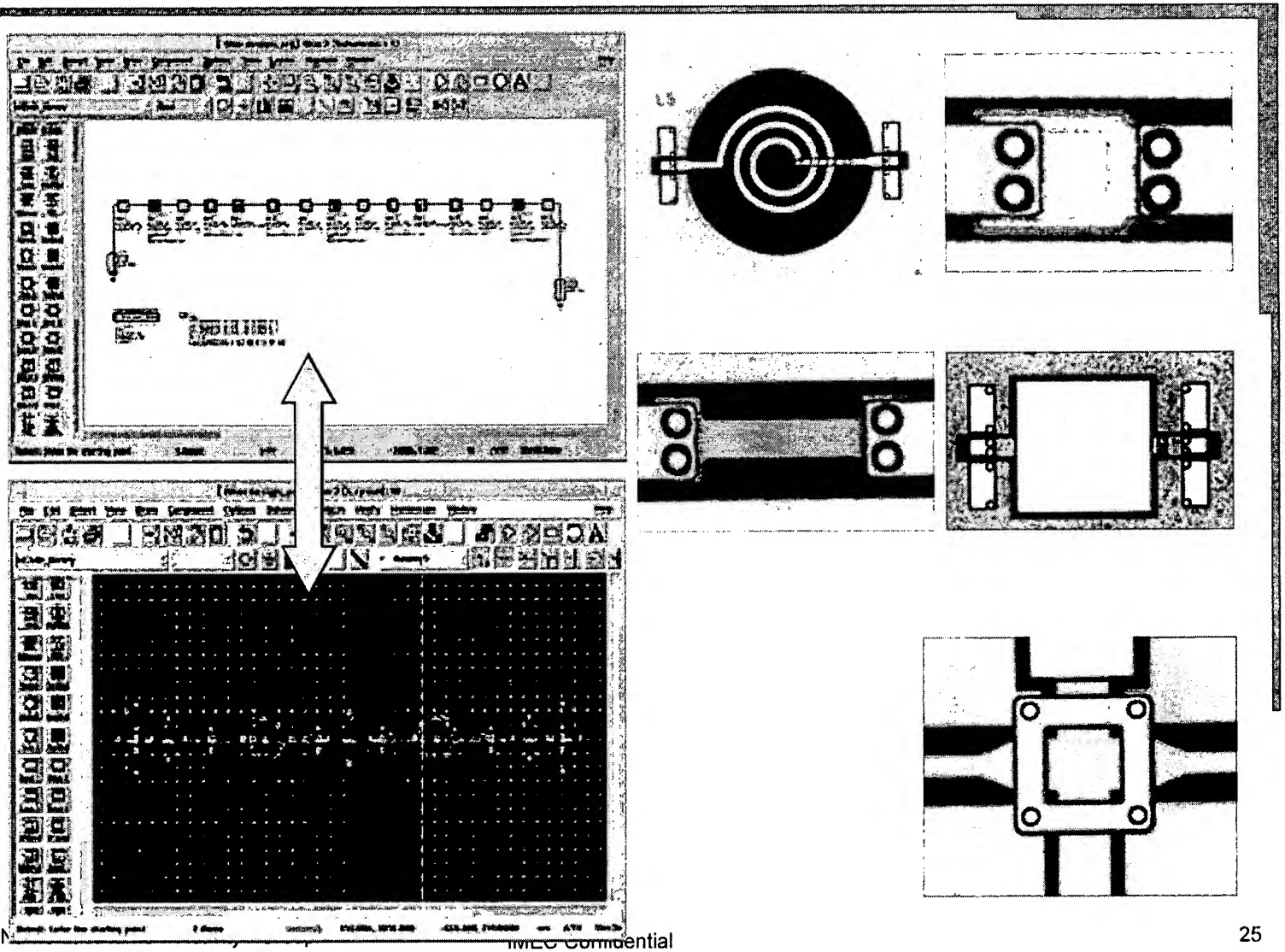
- Coplanar lines
- Electroplated Cu lines (3-5 μm)
- Resistors : TaN (25 Ω/□),
  Ti(O)N (0.5-1 kΩ/□)
- Capacitors : Ta_2O_5 (0.72 nF/mm^2) & BCB (5 pF/ mm^2)
- Inductors : up to 50 nH, Q : 30-150
- Flip chip IC interconnections
- Antenna integration



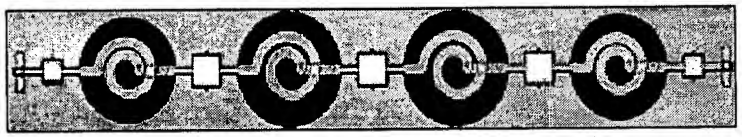




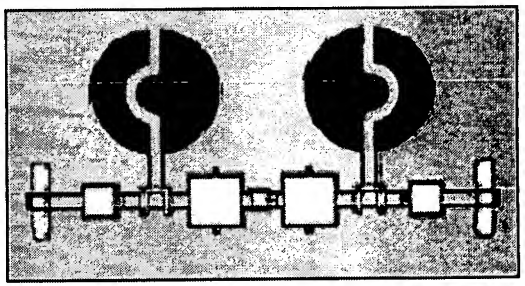
Multilayer thin film with integrated passives



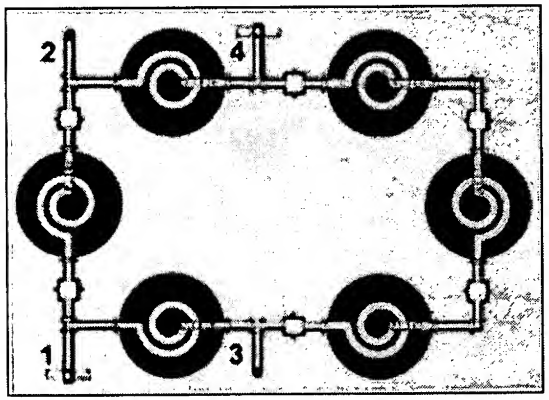
Multilayer thin film with integrated passives



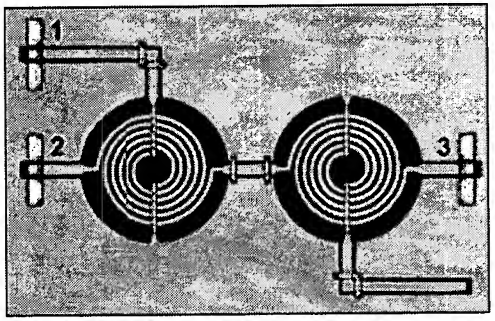
9th order 5.2 GHz Low Pass filter



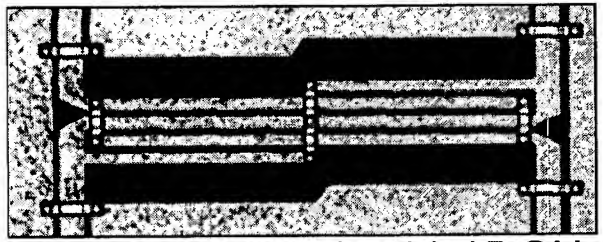
5.2 GHz bandpass filter



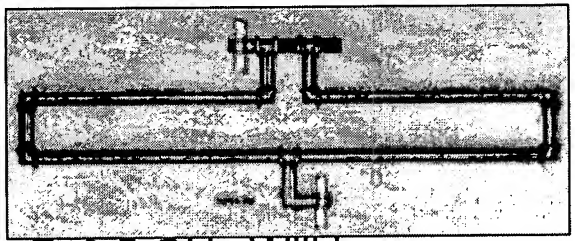
4-6 GHz rat race coupler



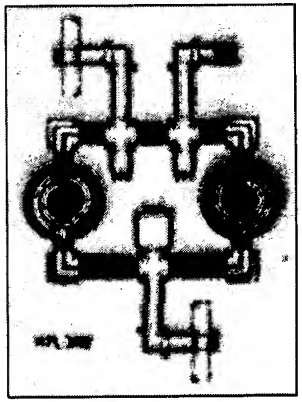
3-5 GHz Balun



CPW Lange coupler 11-15 GHz

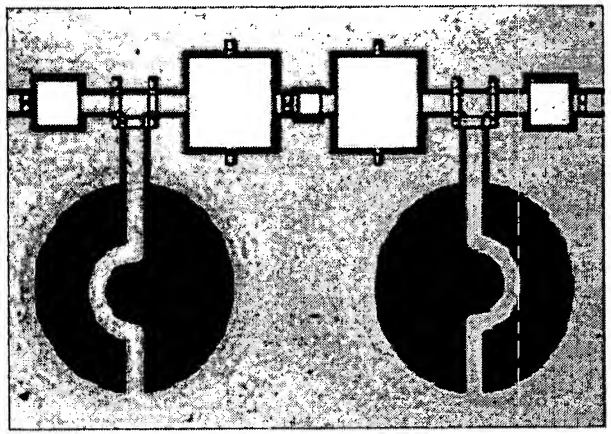


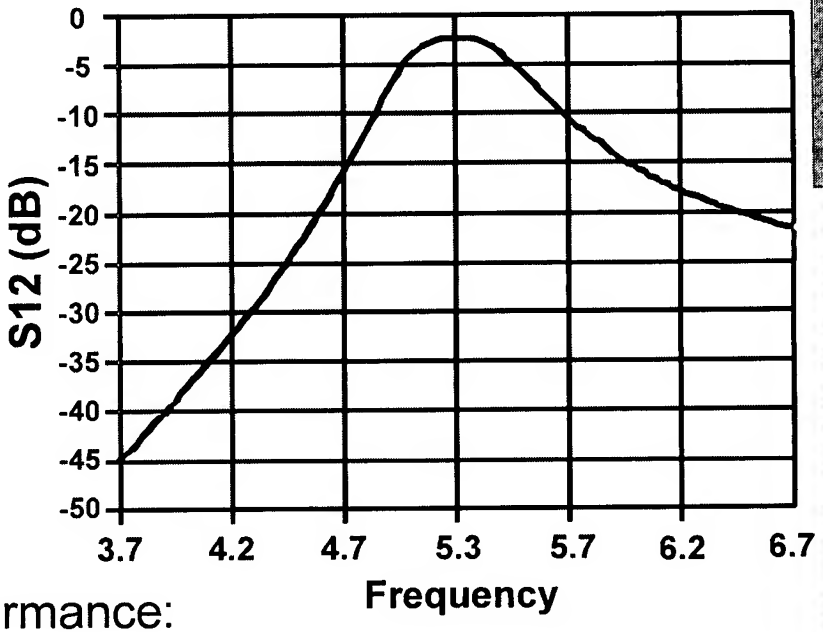
7±0.5 GHz Wilkinson power dividers



Single Package 5 GHz RF receiver front-end

Second order band pass filter





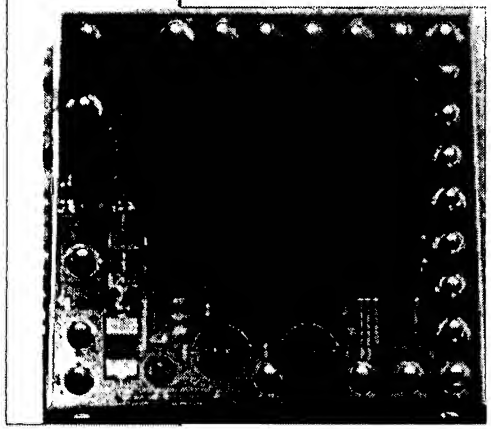
Measured 2nd order BPF performance:

- Insertion loss: 2.4 dB
- Bandwidth: 215 MHz
- Center frequency: 5.2 GHz

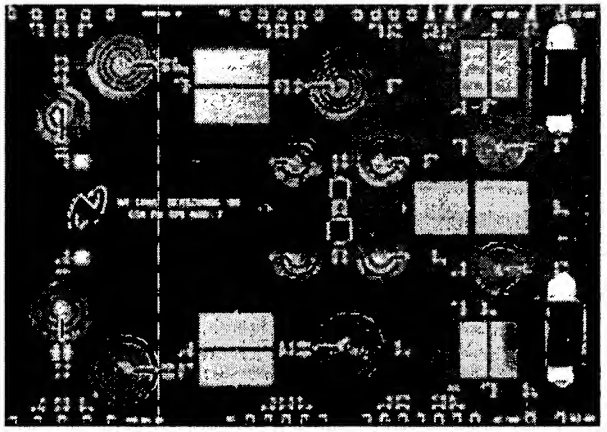
Size: 2.3 mm x 1.4 mm

Multilayer thin film with integrated passives

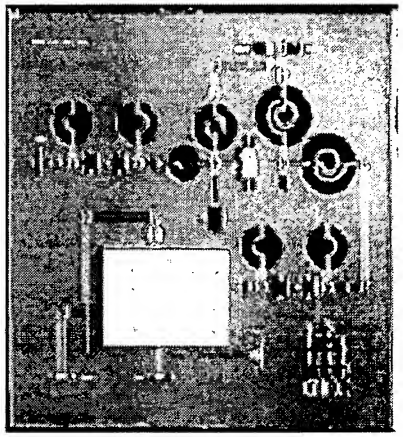
Circuit implementations examples



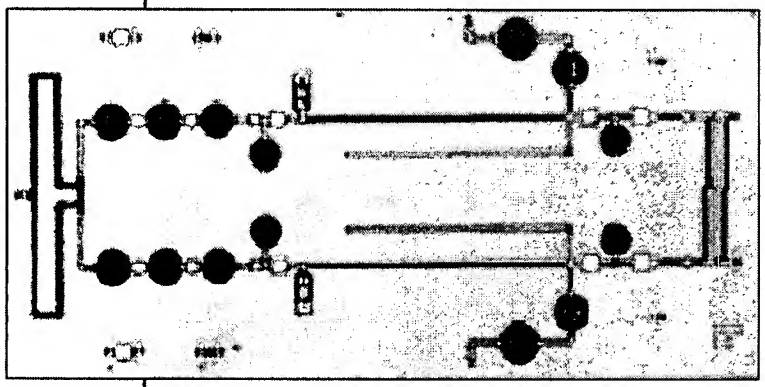
Blue-tooth
Rf circuit



Integrated Passive device
Multiband cell phone Amplifier

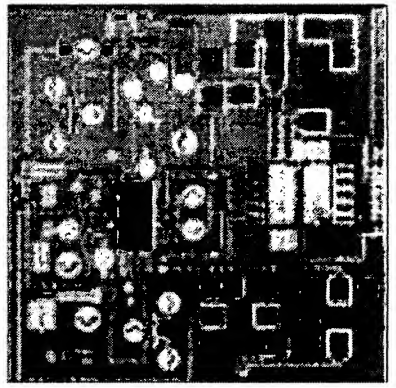


RF s ction
WLAN receiver - 5.2 GHz



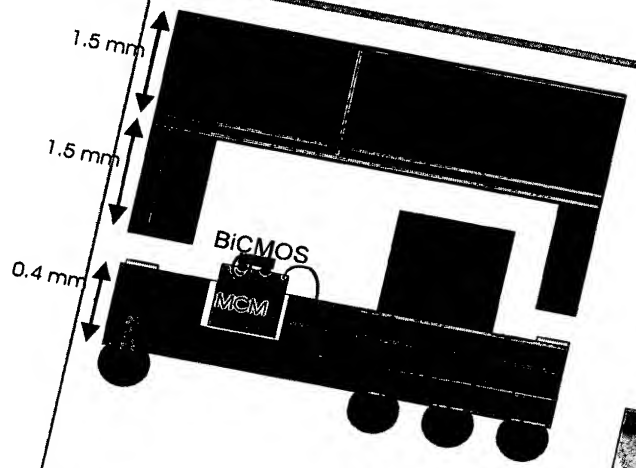
Sub-harmonic
QPSK modulator
LO @ 7 GHz,
RF @ 14 GHz

ALCATEL

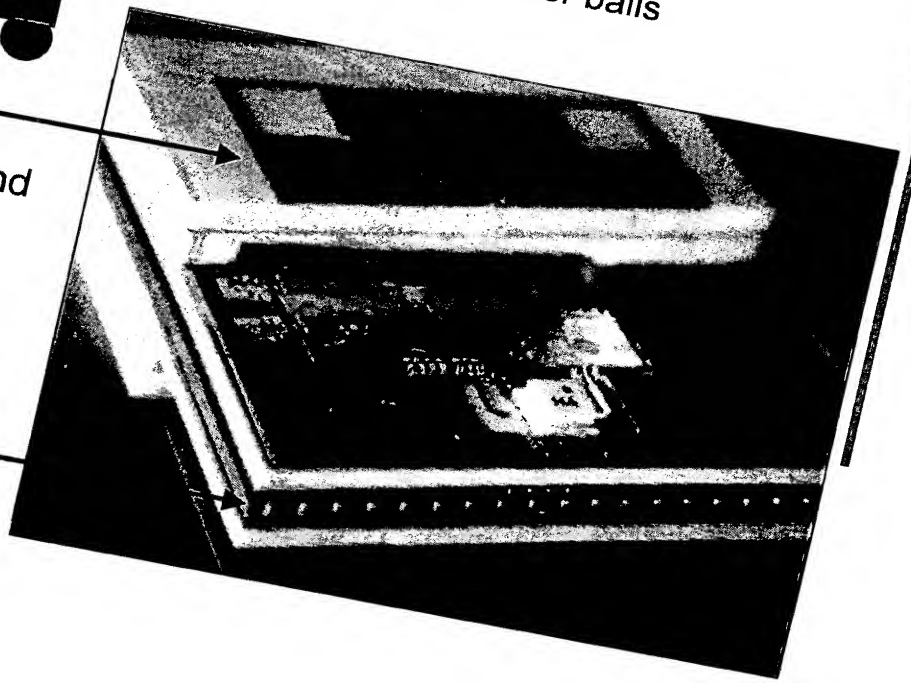


5.2 GHz WLAN front-end

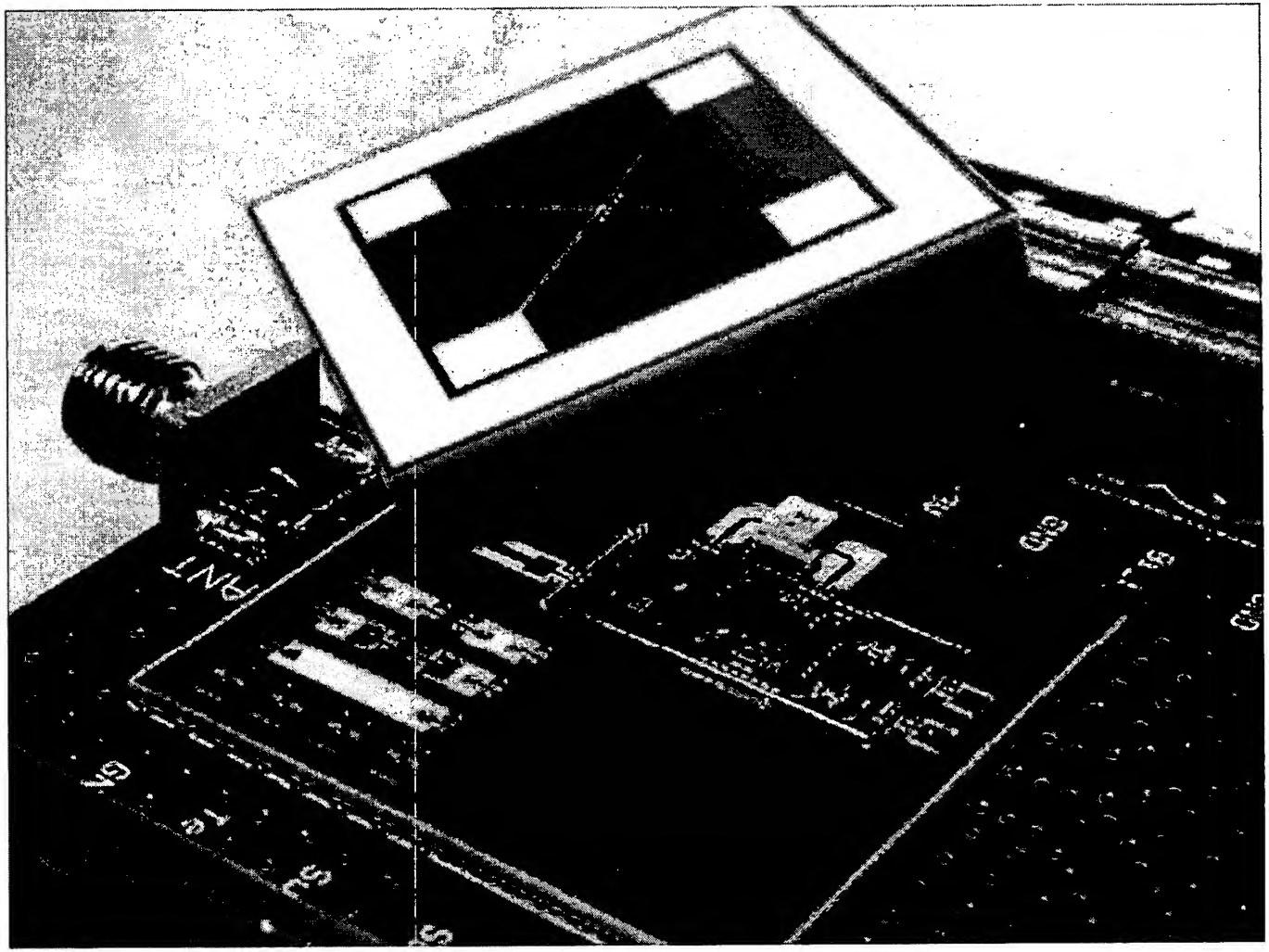
- Antenna layer
- Interconnection layers(feeding)
- Thin film passives layer (MCM)
- Active die layer
- Backside solder balls



Mounting of Antenna and solder ball attachment



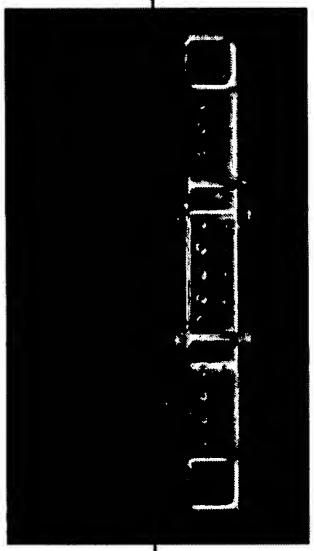
WLAN rf-front end with integrated antenna

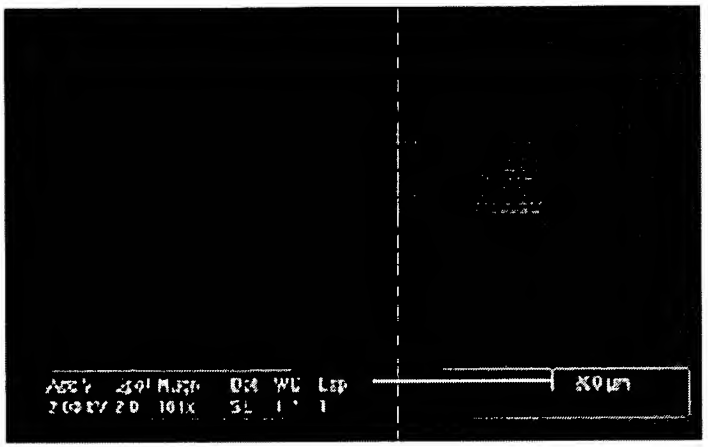


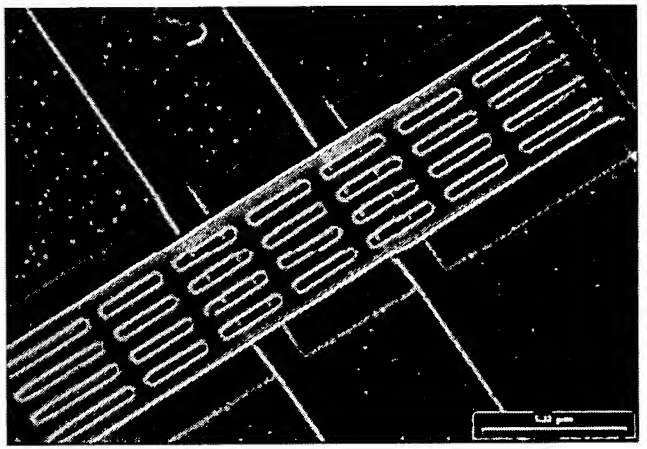
Rf-MCM-D roadmap

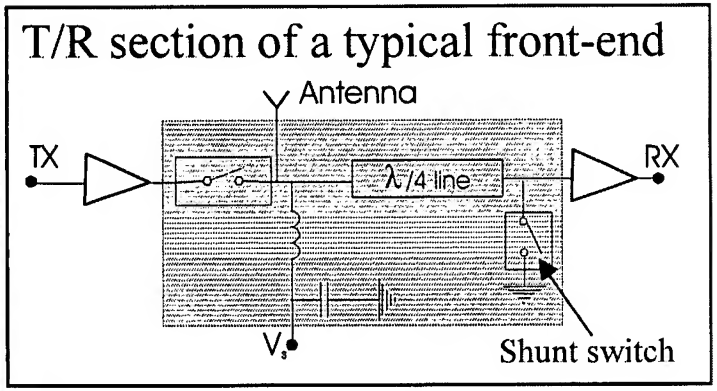
- Further increase of the integration density:
  - Downscaling critical device down to dimensions to 5 μm minimal feature sizes.
- Different substrates :
  - Technology on Si-wafers : high-R Si or using specific wafer preparation to avoid substrate losses
  - Technology on active CMOS Si-wafers : above-IC processing
  - Integrated passives on laminate interposer substrates
- Antenna integration : up to mm wavelengths
- integration rf-MEMS : Rf-MCM_D+

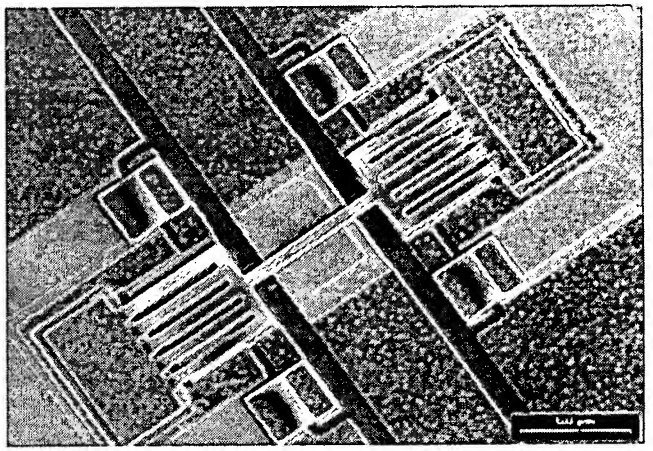
Rf-MEMS Switches



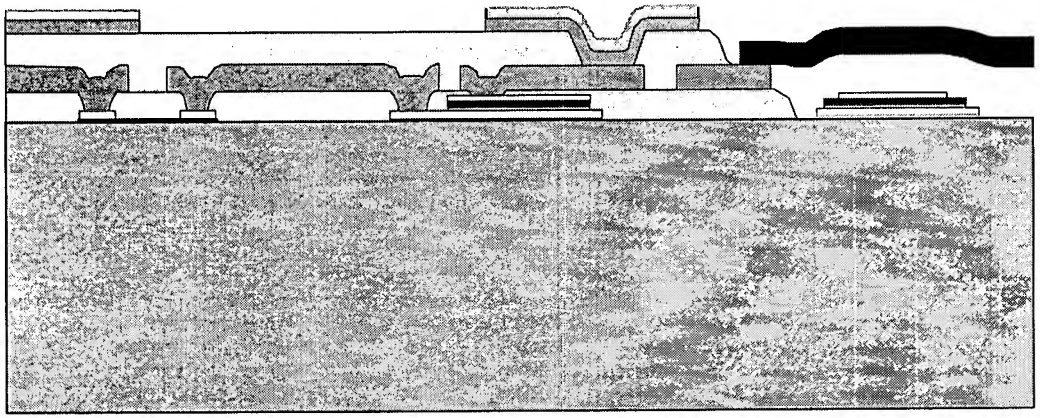




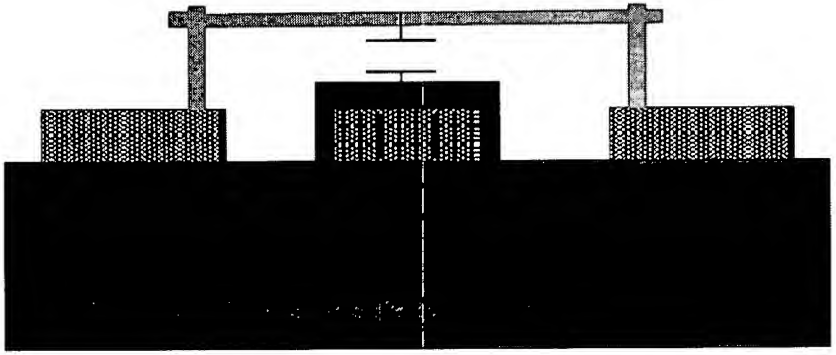




Multilayer Thin Film with Integrated Passives and rf-MEMS



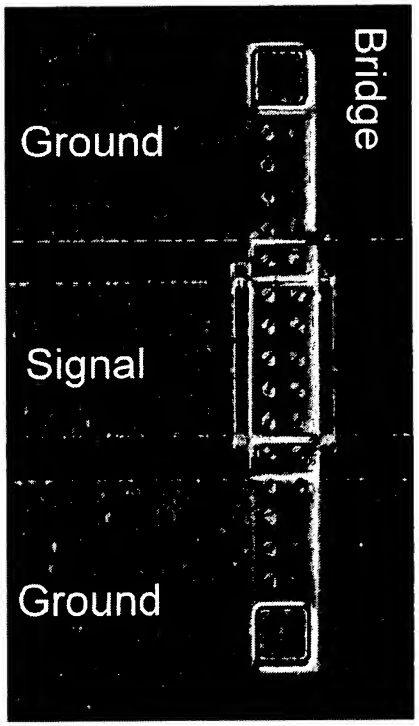
"low" C



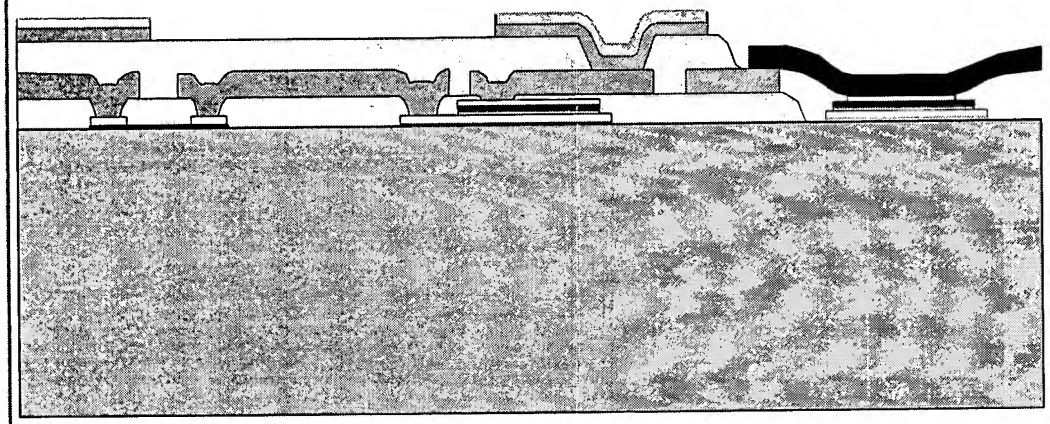
Addition :

Integration of rf-MEMS devices :

Rf-MCM-D+



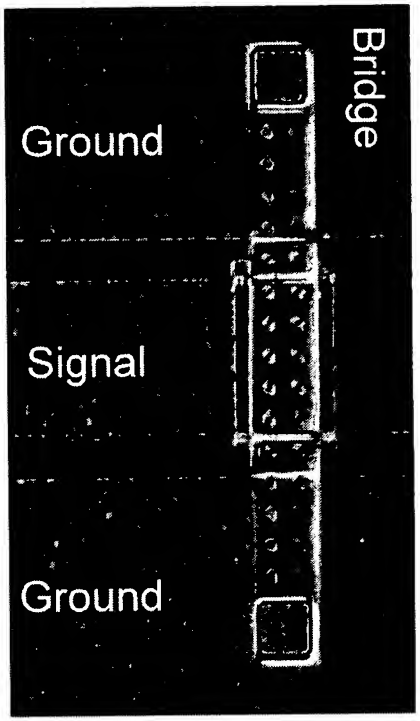
Multilayer Thin Film with Integrated Passives and rf-MEMS



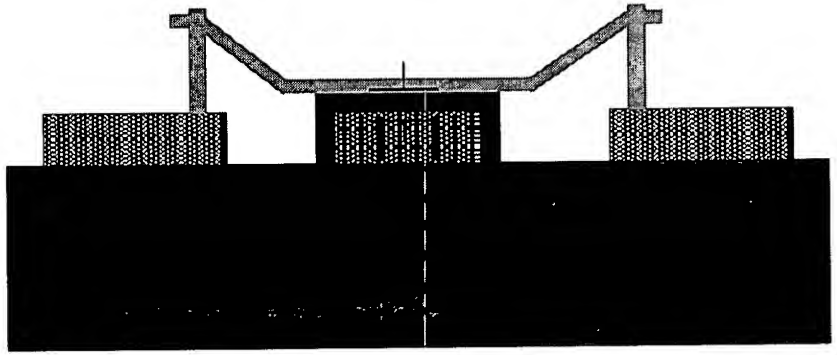
Addition :

Integration of rf-MEMS devices :

rf-MCM-D+



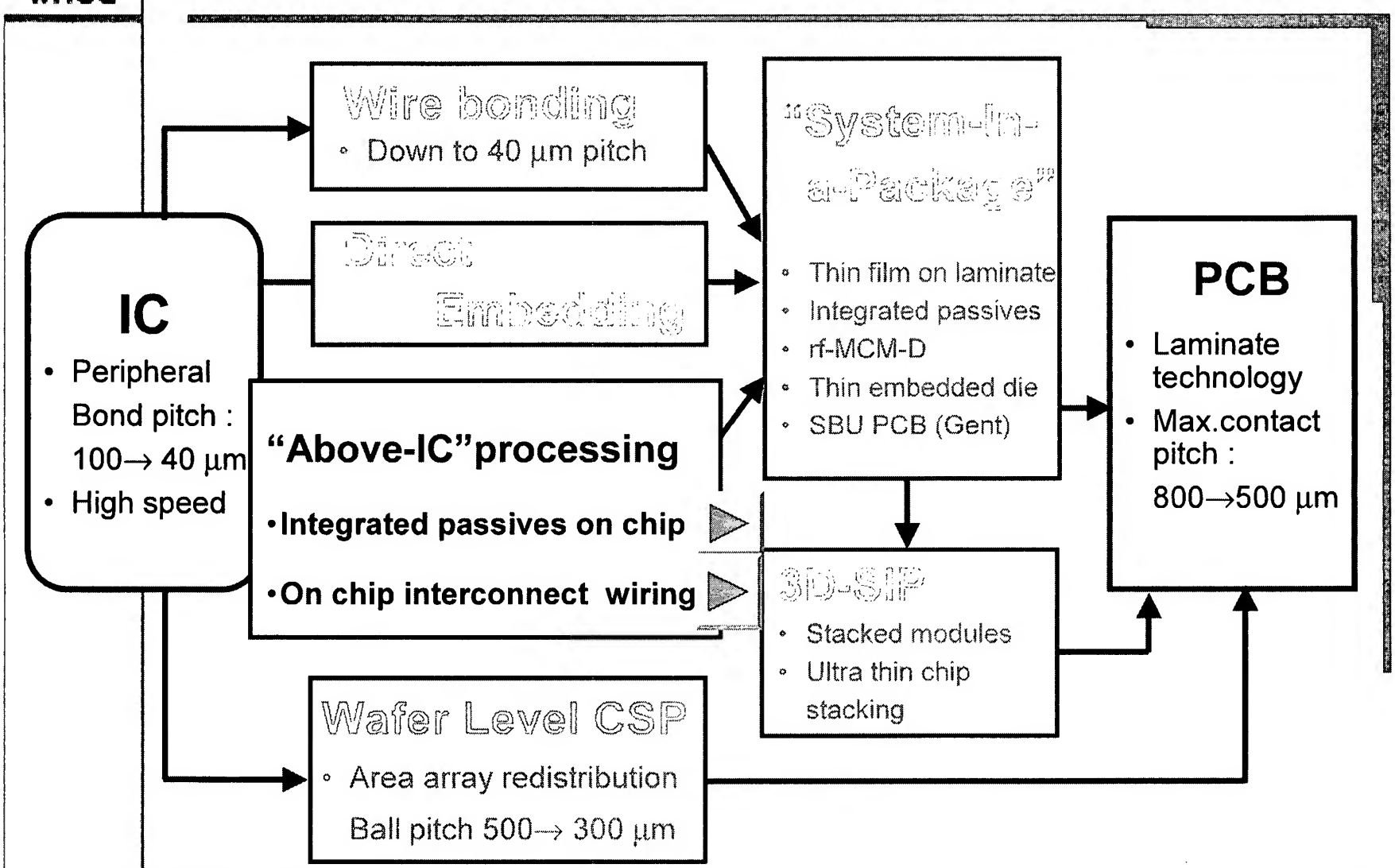
"large" C



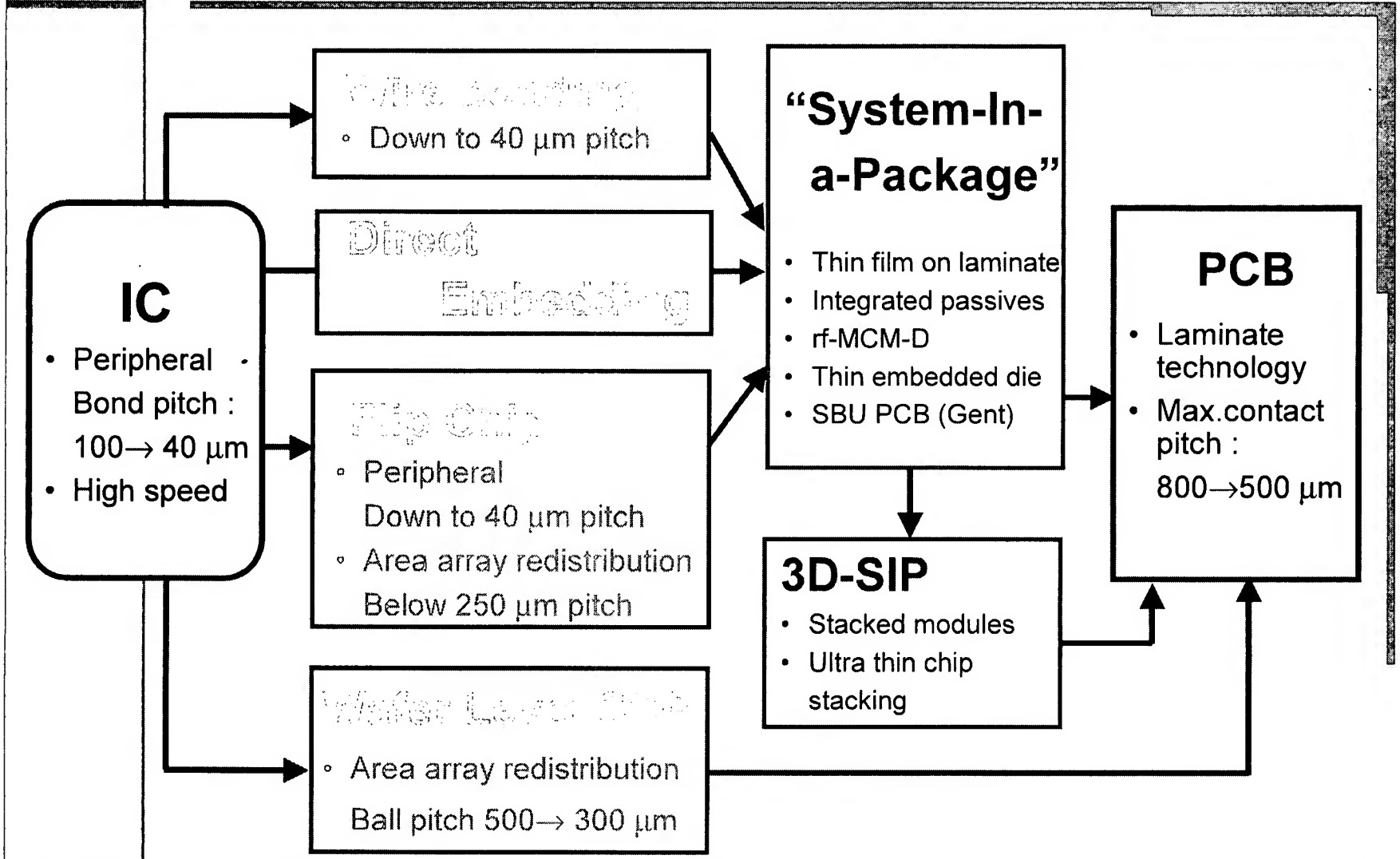
Rf-MEMS roadmap

- Optimisation rf-MEMS switches
  - Higher Con/Coff capacitance ratio
  - Avoidance of sticking during operating live by optimised design and material choice
  - Solutions for Shunt and series switches
- rf-MCM-D+
  - Integration of the rf-MEMS switches in the IMEC rf-MCM-D technology and design library
- Investigation feasibility integration FBAR devices
  - Process compatibility with rf-MCM-D technology
  - Based on Device needs and market requirements
  - Active tuning of the FBAR filter characteristics

Connecting high density IC's

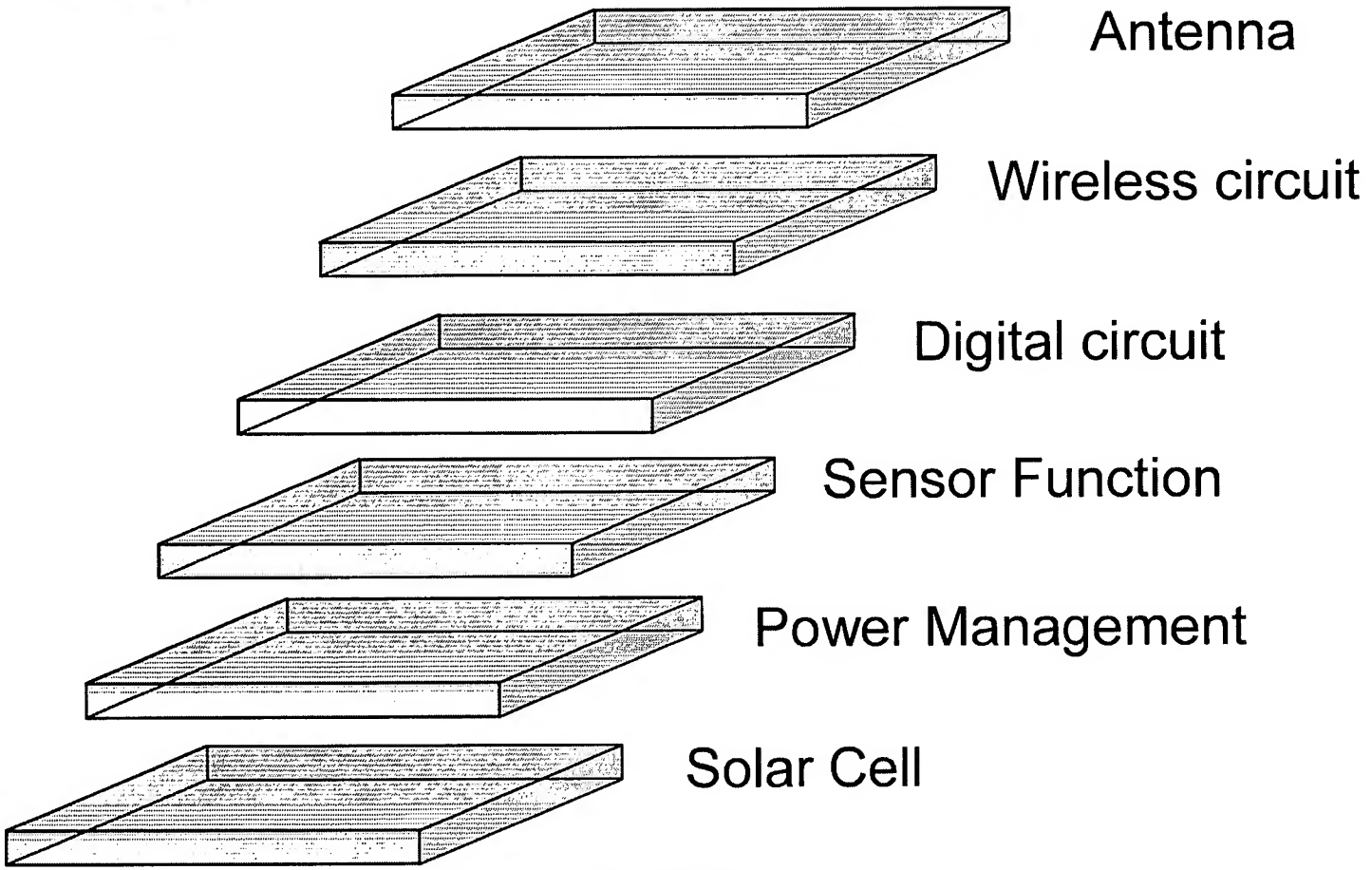


Connecting high density IC's



Miniature, Autonomous Systems

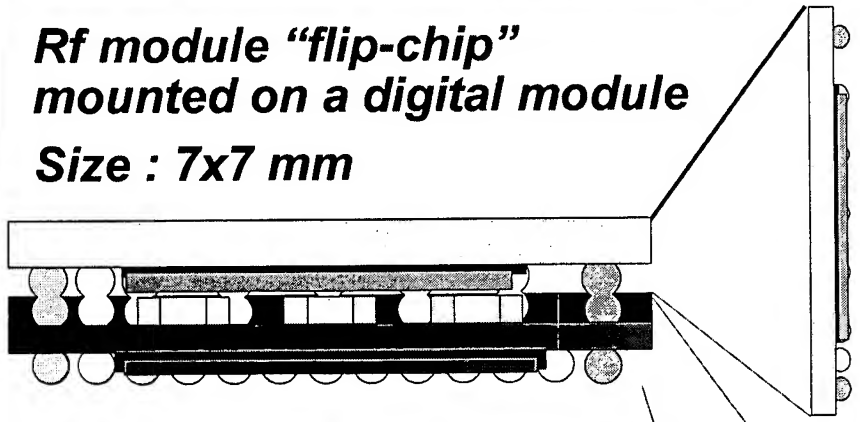
3D- stack of different, miniaturized functional Blocks

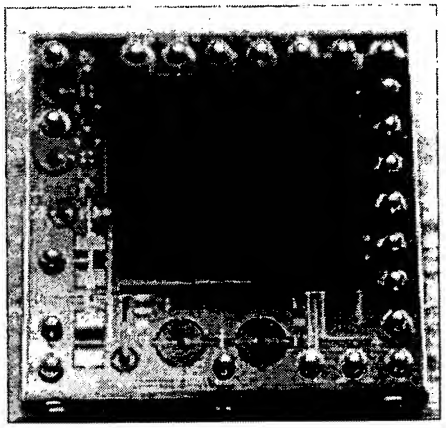


3D fully integrated microwave radio

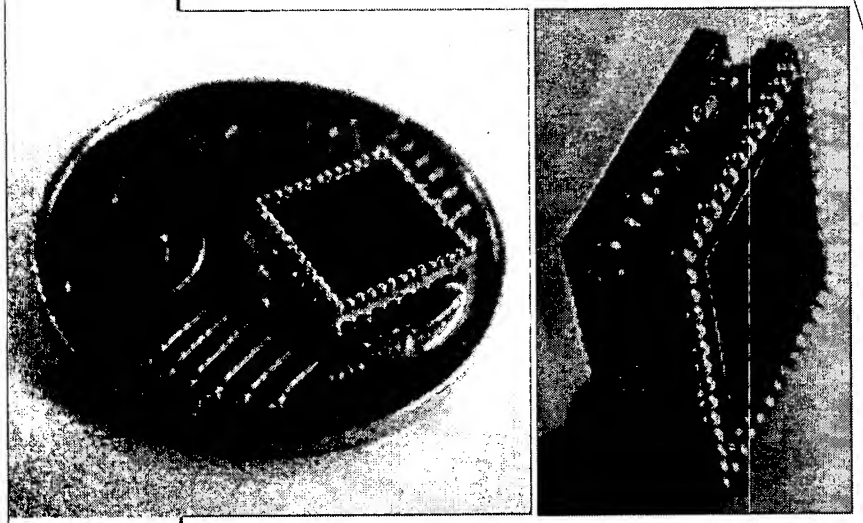
Rf module "flip-chip" mounted on a digital module

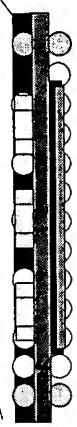
Size : 7x7 mm

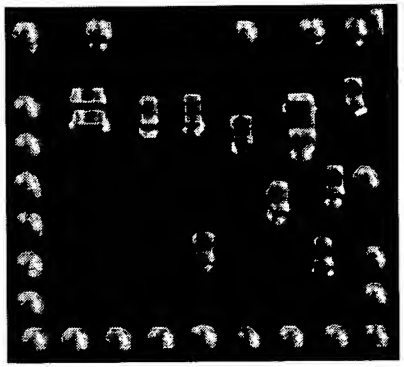




Rf chip "flip-chip" mounted on rf-integrated passives substrate

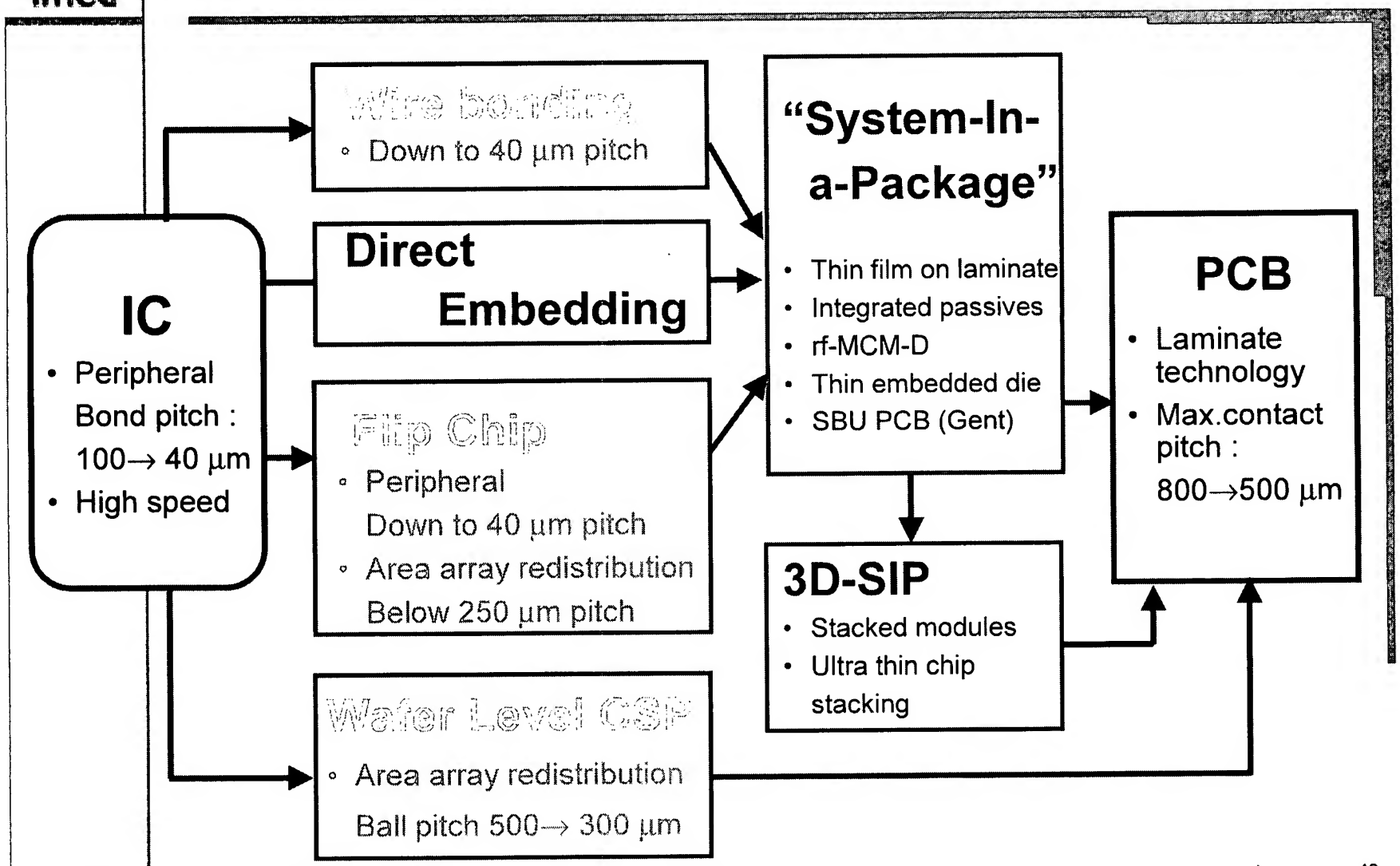






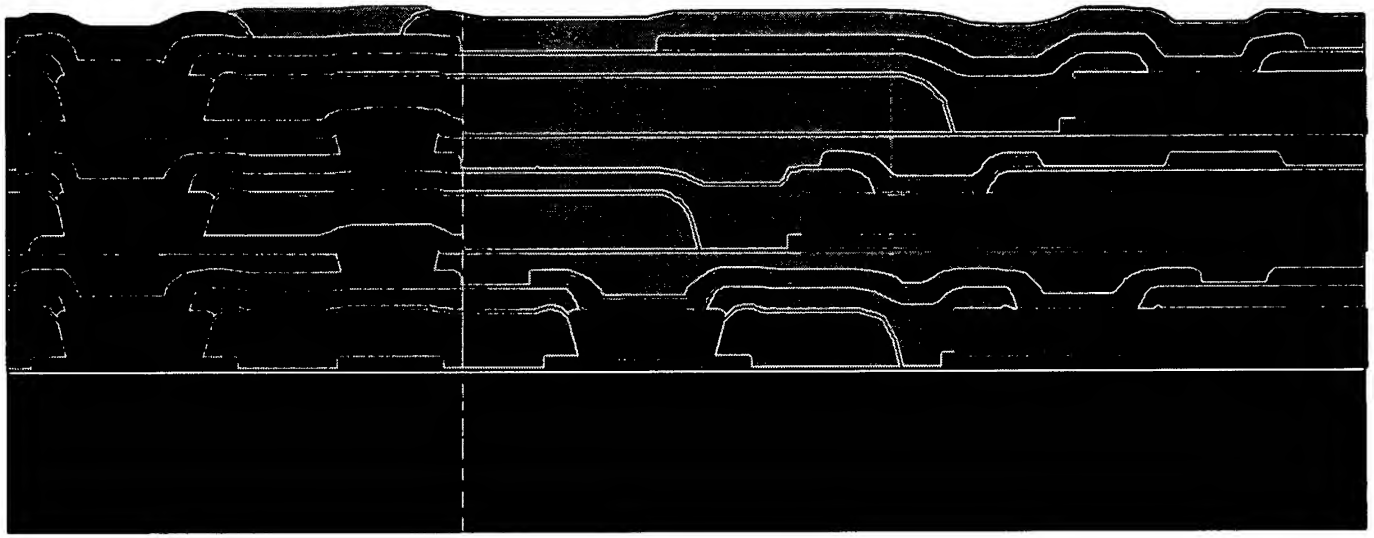
High density laminate with SMD passives on top side and Digital Base band chip on Bottom side

Connecting high density IC's

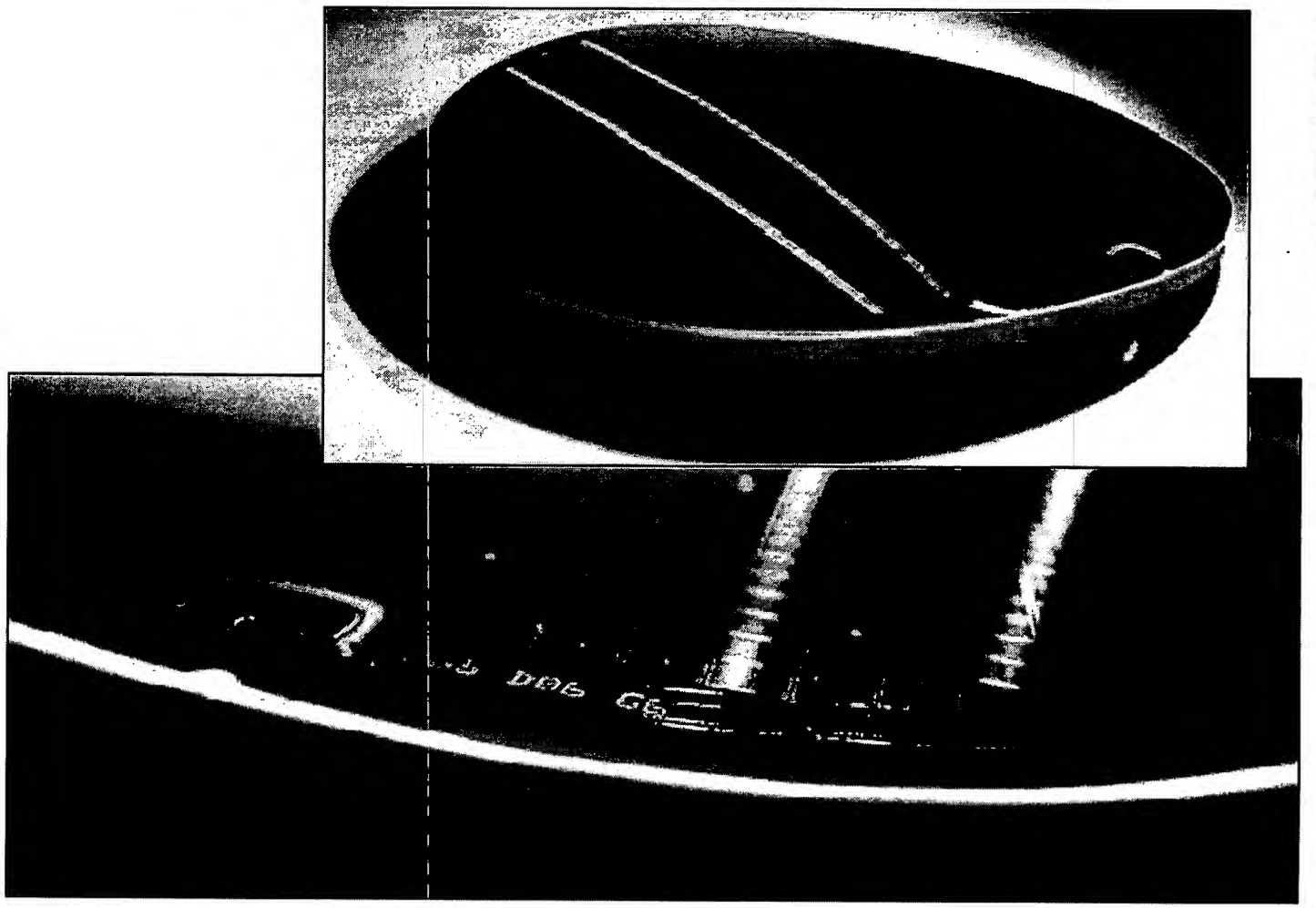


3D- MCM-D : Ultra Thin Chip Stacking (UTCS)

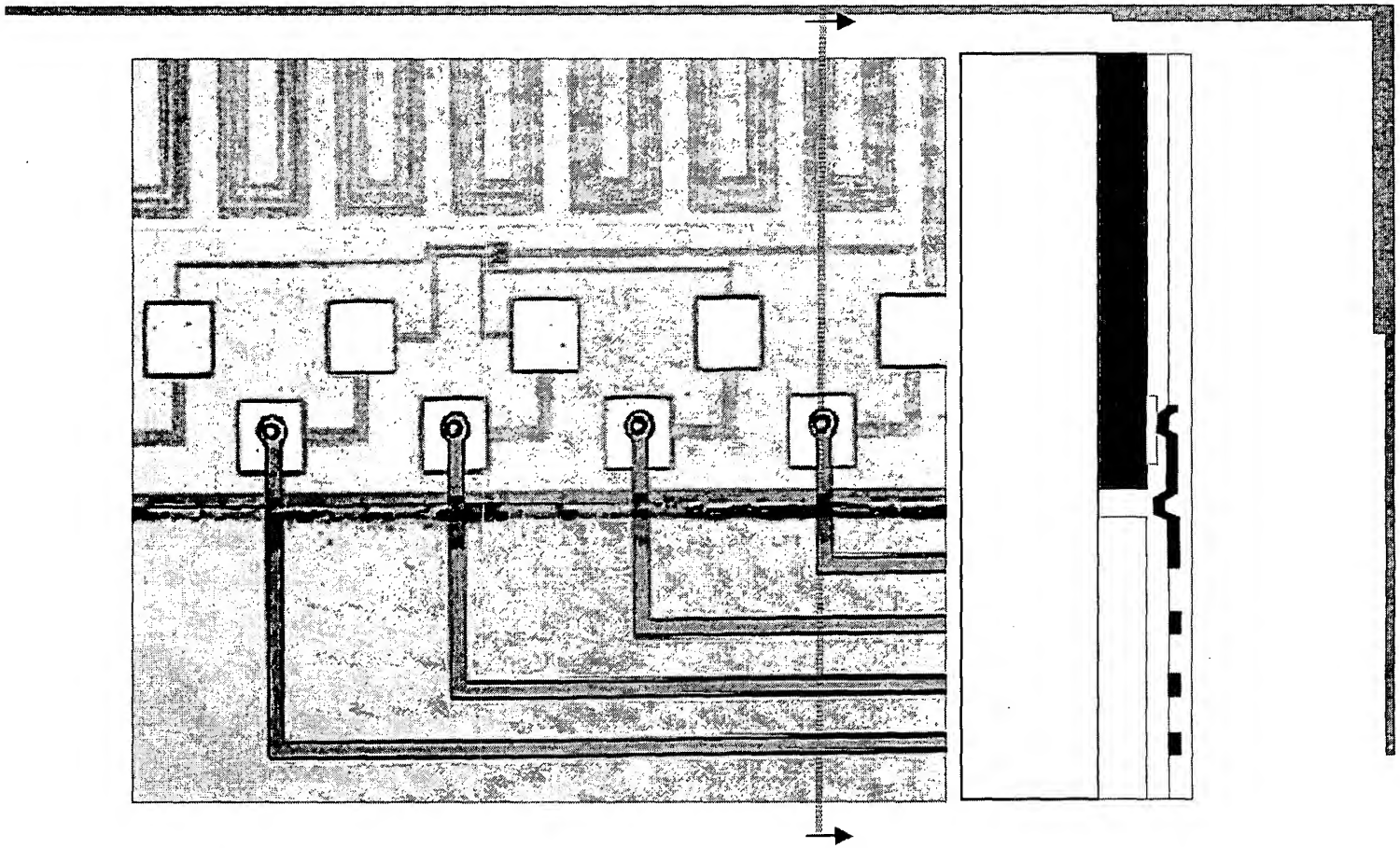
Very thin die (10 μm), embedded in a MCM-D multilayer structure



Wafer thinning :
200 mm wafer thinned to 50 μm by WSI



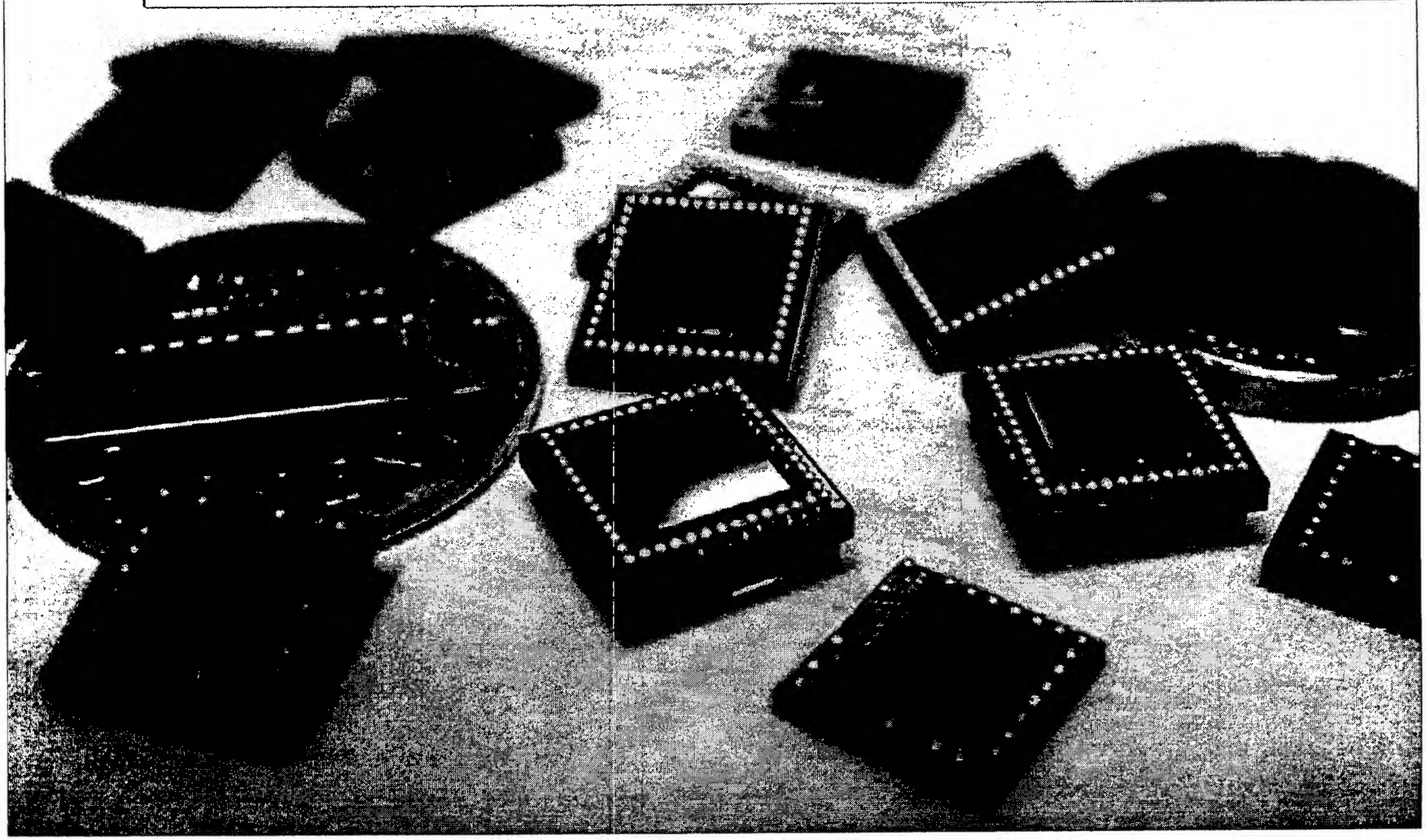
3D-MCM-D : UTCS



Example of a 15 μm thin Si-die, transferred to a host substrate and electrically connected to that substrate

imec

High Density Interconnection and Packaging Research



Industrial Partners in Packaging and High Density Interconnections 2002

Alcatel-Bell, Alcatel-SEL, Alcatel-Space, AMIs, ASM-Pacific, ATMEL, Barco, Bosch, Dane-Elec, Dow Corning, Eltek, Emerson&Cuming, Fiat, Fillfactory, Freudenberg-Mectec, Infineon, Kodak, Matsushita, Motorola, National Semiconductor, Nexx, Nokia, Philips, Rood, Sensornite-Epiq, Septentrio, Siemens Dematic, Sony, SST, ST Microelectronics, Unitron, Xenics